Capacitive Sensor Interface Circuits

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Outline

Introduction

Research Work

Summary
Introduction

Aim and Scope

- Simple capacitive sensor interfaces with focus on:
  1. Straightforward topologies, and
  2. High-density sensor applications
- Highlights:
  1. Current-mode (CM) interface with differential output
  2. Common-source (CS) amplifiers with feedback biasing
- 6 technical papers, 3 on CM approach and 3 on CS amplifiers
Background

Definition

Sensor is:

1. a device that responds to a signal or stimulus.
2. a device that converts a physical phenomenon into an electrical signal.

Introduction

Household appliances: temperature-, humidity-, IR-sensors

AV: acoustical-, optical-sensors
Potential in sensors is widely acknowledged…

Sensor Classification

By measurand/application:
- Temperature
- Pressure
- Flow
- Radiation
- Chemical
...

By output signal:
- Active
- Passive
...

By measurement principle:
- Resistive
- Capacitive
- Inductive
- Piezoelectric
...

“I was selling lemonade, but I soon realized there’s better money in wireless sensors.”
Background

1. Credit goes to CMOS technology due to
   – flexible and versatile DSP
   – rapid and constant pace of development
   – cheap fabrication

2. Digital processing is mostly used, but analog is still required because
   – the real world is analog
   – sensor output needs to be conditioned

Sensor Signal Conditioning
Capacitive Sensors

Capacitance formula

\[ C = \epsilon \frac{A}{d} \]

- Passive
- Several advantages:
  - No DC bias
  - Compatible with CMOS
  - Non-contact measurement
  - High immunity
  - ...
- Popular in MEMS and micro-sensors
- Differential or single-ended

Capacitive Sensors – Plate Distance Sensing

- Single-ended: (a)–(b)
- Differential: (c)–(d)
- Advantages (differential):
  - Common-mode rejection
  - ΔC sensing
- Disadvantages (differential):
  - Expensive
CMUT: An Application of Capacitive Sensing

- A transducer
- Compatible with CMOS
- Can be used in immersed media

**Advantages:**
- Local signal-cond.
- Dense arrays possible
- Can be tailor made

**Challenges:**
- Compact circuitry
- Power efficiency

Interface Circuits for Capacitive Sensors

1. High-Z sensing
   - Norton equiv. (a)
   - Simple to implement in CMOS
   - Most efficient topologies available
   - Not seen much for CMUT interface

2. Low-Z sensing
   - Thévenin equiv. (b)
   - Mostly used for CMUT interface

3. Feedback assisted sensing
   - Improves linearity
   - Usually more complex
In a Nutshell ...

1. There is a steady growth in sensor applications
2. Capacitive sensing is popular in many modern sensors
3. CMUTs use capacitive sensing in receive mode
4. Area and efficiency are important in dense sensor arrays
5. Voltage sensing may be used to meet such goals

Research Work
The Current-Mode Approach

Paper 1
A Single-Ended to Differential Capacitive Sensor Interface Circuit Designed in CMOS Technology
Tajeshwar Singh and Trond Ytterdal

In proceedings of:

Paper 4
Current Mode Capacitive Sensor Interface Circuit with Single-Ended to Differential Output Capability
Tajeshwar Singh, Trond Sæther and Trond Ytterdal

Accepted for publication in:

Salient Features

- Differential output, also from a single-ended sensor
- Simply realized with standard analog building blocks
- Requires that both sensor and reference capacitances are ungrounded
- Realized in AMS’ 0.8-µm CMOS technology
Measurement Concept

\[ V_{dd} \]

\[ I_b \]

\[ I_1 = \frac{I_b}{2} + \frac{i}{2} \]

\[ I_2 = \frac{I_b}{2} - \frac{i}{2} \]

\[ I_1 = (C_m + C_r) \frac{dV_1}{dt} \]

\[ V_{out} = V_{op} - V_{om} = iR_f = R_f \frac{\Delta C}{2(C + \Delta C)} \]

Parasitics Influence

\[ V_{dd} \]

\[ I_b \]

\[ i = \frac{I_b \Delta C}{2C + \Delta C + C_p} \]

\[ V_{DD} \]

\[ I_b \]

\[ i = \frac{2I_b \Delta C}{2C + C_p} \]
Transfer Function – Single Ended Sensor

\[ V_{out} = R_f I_b \frac{\Delta C}{C + \Delta C} \]

\( R_f = 200 \, \text{k}\Omega, \, I_b = 2.5 \, \mu\text{A}, \, C = 1 \, \text{pF} \)

Circuit Realization
Transient Response

Chip Photograph
Measurement Results

Summary of Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal value of $C_m$ and $C_r$</td>
<td>1 pF</td>
</tr>
<tr>
<td>Capacitance range ($\Delta C$)</td>
<td>0.75 pF</td>
</tr>
<tr>
<td>Value of feedback resistors $R_f$</td>
<td>200 k,\Omega</td>
</tr>
<tr>
<td>Charging current $I_b$</td>
<td>2.5 , \mu A</td>
</tr>
<tr>
<td>Output swing</td>
<td>136.4 mV</td>
</tr>
<tr>
<td>Measurement uncertainty due to noise (simulated)</td>
<td>1.13 fF</td>
</tr>
<tr>
<td>Maximum non-linearity error relative to full-scale swing</td>
<td>0.17% (no stray capacitance) 0.67% (with 0.25 pF stray cap.)</td>
</tr>
<tr>
<td>Current consumption</td>
<td>145 , \mu A (without buffers)</td>
</tr>
</tbody>
</table>
Measurement Results – contd.

Comparison with other work

<table>
<thead>
<tr>
<th>Parameter</th>
<th>[BMPH07]</th>
<th>[DKPS06]</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Error</td>
<td>0.2%</td>
<td>0.8%</td>
<td>0.7%</td>
</tr>
<tr>
<td>Area</td>
<td>9.3 mm²</td>
<td>NA</td>
<td>2.2 mm²</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>120 µW</td>
<td>50 µW</td>
<td>725 µW</td>
</tr>
<tr>
<td>CMOS Technology</td>
<td>0.5-µm</td>
<td>0.35-µm</td>
<td>0.8-µm</td>
</tr>
</tbody>
</table>

The Current Mode Approach Modified

Paper 2

A Linear Capacitive Sensor Interface Circuit with Single-Ended to Differential Output Capability

Tajeshwar Singh, Trond Sæther and Trond Ytterdal

In proceedings of:
The NORCHIP Conference 2004.
Salient Features

- A method to remove the influence of parasitic capacitance
- Pseudo-Differential output (with single-ended sensor)
- Proportional to $\Delta C$
- Simulated in AMS’ 0.35-$\mu$m CMOS technology

Measurement Concept

\[ i = \frac{I_b \Delta C}{2C + \Delta C + C_p} \]

\[ V_1 = a I_t \]

\[ I_m = C_m \cdot a \]

\[ I_r = C_r \cdot a \]

\[ i = a \cdot \Delta C \]
Realization

\[ V_{\text{out}} = \Delta C \cdot R_f \cdot \frac{dV_1}{dt} = \Delta C \cdot R_f \cdot \alpha \]

Simulations

(\(R_f = 150 \, \text{k} \Omega\), \(C = 1 \, \text{pF}\), \(\Delta C_{\text{max}} = 0.5 \, \text{pF}\))

Plots shown for \(C_m = 1.2 \, \text{pF}\) and \(1.5 \, \text{pF}\)
Feedback Biasing in Nanoscale CMOS Technologies

Papers

Common Source Amplifier with Feedback Biasing in 90nm CMOS
In proceedings of:
The IEEE PRIME’06.

Feedback Biasing in Nanoscale CMOS Technologies
Published in:
IEEE Transactions on Circuits and Systems—Part II: Express Briefs.

Compensating for Non-Linearity in Feedback Biased Common-Source Amplifiers Using MOS Feedback Resistors
Submitted to:

– Tajeshwar Singh, Trond Sæther and Trond Ytterdal

Salient Features

- A very compact biasing method
- Exploits some of the limitations of nanoscale technologies
- Suited for applications where bandpass amplifier response is acceptable
- Extremely compact amplifiers can be realized
Feedback Biasing – Output Swing

\[ v_{\text{OUT}_{\text{min}}} \equiv v_{\text{DS_MIN}} \approx v_{\text{GS_MAX}} - V_T \]

\[ v_{\text{OUT}_{\text{min}}} \approx \frac{V_{\text{DD}} - V_{\text{SS}}}{2} - V_T \]

Non-Proportional Scaling

Feedback Biasing – Frequency Response

\[ LG(s) = \frac{v_f(s)}{v_i(s)} = g_m \cdot \frac{R_{\text{out}}}{1 + sR_{\text{out}}C_L} \cdot \frac{1 + R_GC_G}{1 + R_G(C_G + C_{\text{IN}})} \]

\[ \omega_3 = \frac{g_mR_{\text{out}}}{R_G(C_G + C_{\text{IN}})} \approx \frac{g_mR_{\text{out}}}{R_GC_{\text{IN}}} \]

\[ \omega_{3dB} = \frac{1}{R_{\text{EQ}}C_{\text{IN}}} \approx \frac{1 + g_mR_{\text{out}}}{R_GC_{\text{IN}}} \]

Cascaded CS Amplifier with Feedback Biasing
Prototype in 90-nm CMOS

Simulations and Measurements

![Frequency and Gain Graph](image)

- Frequency [Hz]: $10^4$, $10^5$, $10^6$, $10^7$, $10^8$
- Gain [dB]: 5, 10, 15, 20, 25, 30, 35

Simulated - Measured
Simulations and Measurements – contd.

Summary of Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Type / Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage gain at 30 MHz</td>
<td>28.5 dB</td>
</tr>
<tr>
<td>Gain variation within pass-band (20 MHz–50 MHz)</td>
<td>0.4 dB</td>
</tr>
<tr>
<td>Output DC level</td>
<td>0.577 V</td>
</tr>
<tr>
<td>Output noise PSD at 30 MHz</td>
<td>0.14 (µV)²/Hz</td>
</tr>
<tr>
<td>THD at FS output at 30 MHz</td>
<td>−26.33 dB</td>
</tr>
<tr>
<td>Input impedance (RC)</td>
<td>R = 6 M1 C = 7 pF</td>
</tr>
<tr>
<td>Current consumption (1-V power supply)</td>
<td>120 µA (without biasing current mirror)</td>
</tr>
<tr>
<td>Area</td>
<td>20 µm × 10 µm</td>
</tr>
</tbody>
</table>

Non-Linearity

![Non-Linearity Diagram](image-url)
Non-Linearity Reduction

Linearity Performance – Simulations and Measurements
Summary

- Feedback biasing has been revived in nanoscale technologies
- Some of the limitations of nanoscale technologies can be exploited
- A simple way to generate differential output from a single-ended sensor was demonstrated

Future Work

- Current-mode capacitive interface in nanoscale CMOS
- Proof-on-silicon and further work on the linear interface
- Application of feedback biasing to other circuits