HIGH SPEED INTERLEAVED SAR ADC FOR OPTICAL COMMUNICATIONS

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Presentation for Course Data Converter
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PAPERS

- Paper 1
  A 24GS/s 6b ADC in 90nm CMOS
  Authors: P Schvan et. al. ISSCC 2008

- Paper 2
  A 40GS/s 6b ADC in 65nm CMOS
  Authors: Greshishchev, Y.M. et. al. ISSCC 2010
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**BACKGROUND**

- Application in receivers for 10-to-40Gb/s optical communications, which uses DSP-based equalization.
  - Require a 6b ADC
  - Sampling frequency higher than 24GS/s
  - Low ENOB degradation over 4 up to 8GHz
  - Advanced CMOS technology

- Paper 1 presents a 24GS/s 6b ADC in 90nm CMOS with the highest ENOB up to 12GHz input frequency and lowest power consumption of 1.2W.
ADC Architecture

- Use an interleaved architecture of SAR type converters.
  - High-speed interleaved ADC can be realized by operating many lower speed ADCs in parallel.
  - Requires Offset, Delay and Gain correction

- Paper 1 uses 16 interleaved 25mW 1.5GS/s 6b sub-ADCs operating from 1V supply, proceeded by an array of 2.5V T/Hs.
ADC Architecture

- 16 sub-ADCs
- T/H array is split into 2.
- Power splitter at the 50Ohm input
- Calibration array
- DeMux

Figure 30.3.1: ADC architecture including on-chip memory for testing.
CRITICAL COMPONENTS
TRACK AND HOLD CIRCUIT (1/3)

- T/H circuits:
  - Differential nmos transfer gate
  - Dummy transistors: avoid kickback noise
  - Feedthrough compensation

Figure 30.3.2: Schematic of the T/H and CML to CMOS converter.
CRITICAL COMPONENTS TRACK AND HOLD CIRCUIT (2/3)

- CML: Current mode logic for high speed circuit
  - Smaller output swings
  - Constant static power
  - Smaller dynamic power
  - The constant supply currents, lower cross talk.
  - Keeping the power supply noise at a low level.

Figure 30.3.2: Schematic of the T/H and CML to CMOS converter.
CRITICAL COMPONENTS
TRACK AND HOLD CIRCUIT (3/3)

- 1V CML to 2.5V CMOS clock converter
  - Two differential amplifiers (M11-M18)
  - Pull-up current sources M9-M10: Provide biasing; Decrease sensitivity to noise
  - Resistors R1, R2 improve frequency response.

Figure 30.3.2: Schematic of the T/H and CML to CMOS converter.
**Critical Components**  
**Multi-phase Clock Generation (1/2)**

- The multi-phase 1.5GHz sampling clocks are generated by clocking two sets of shift registers with both edges of the $F_s/4=6$GHz I,Q quadrature clocks.

- The delay of each sampling clock is fine tuned in 0.4ps steps using a phase interpolator.

*Figure 30.3.3: Multi-phase clock generator.*
Sampling clock diagram
1.5GS/s 25% duty cycle
CRITICAL COMPONENTS

SUB-ADC

- 25mW, 6b, 1.5GS/s
- The sub-ADC is composed of 10 elementary SAR converters running in parallel at full clock rate.
- 10 clock cycles for each single SAR converter:
  - 2 for the self-calibration
  - 1 for input signal sampling
  - 6 for the bit cycling
  - 1 for data output delivery.
- The overall output data rate equals the clock rate.
ADC Output Spectrum

- Before calibration, output spectrum typically shows largest spurs related to the input frequency mixed with harmonics of 1/16th and 1/4th of the sampling clock frequency.
- After the calibration, maximum harmonic power (SFDR) is < -35dBc up to Fin=12GHz or about -50dBc for Fin=3.28GHz.

Figure 30.3.5: ADC output spectrum (a) before and (b) after calibration.
ENOB vs. Input Frequency

- Two ways:
  (a) Averaged calibration settings.
  (b) Calibration is re-done at each frequency.
- ENOB remains above 4.1 up to 8GHz and above 3.5 up to 12GHz input frequency.
- The reduction of ENOB at higher frequency is due to clock jitter, uncompensated timing skew and T/H non-linearity.
### Comparisons of High Speed ADCs

<table>
<thead>
<tr>
<th>Paper</th>
<th>Fs</th>
<th>Resolution</th>
<th>Technology</th>
<th>Power</th>
</tr>
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<tbody>
<tr>
<td>Nosaka ’04</td>
<td>24Gs/s</td>
<td>3b</td>
<td>InP</td>
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<tr>
<td>Schvan ’06</td>
<td>22GS/s</td>
<td>5b</td>
<td>BiCMOS</td>
<td>3W</td>
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<tr>
<td>Poulton ’03</td>
<td>20GS/s</td>
<td>4.6b</td>
<td>0.18um</td>
<td>9W</td>
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<td>Lee ’03</td>
<td>10GS/s</td>
<td>5b</td>
<td>SiGe BiCMOS</td>
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<tr>
<td>Harwood ’07</td>
<td>12.5GS/s</td>
<td>4.5b</td>
<td>65nm</td>
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<tr>
<td>This work</td>
<td>24GS/s</td>
<td>6b</td>
<td>90nm</td>
<td>1.2W</td>
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</tbody>
</table>
COMPARISONS OF HIGH SPEED ADCs

FoM = \frac{P}{2F_{\text{in}} 2^{\text{ENOB}}}

Sampling rate, GS/s

FoM, pJ/conv.

[Lee'03] [Poulton'03] [Schvan'06]
[Nosaka'04] [Harwood'07] This work
Challenges:
- Sampling rate of 29GS/s
- Sub-ADC consumes < 40mW at 2.5Gs/s @ 1V power supply.
- 65nm technology
T/H CIRCUIT FOR PAPER 2

- Implemented with 1V and 1.2V MOS devices simplifying the switch topology.
- Only clock feedthrough is now compensated (M3, M4).
- The CML to CMOS converter is also simplified, while producing 1.2V CMOS swing.

Figure 21.7.3: Schematic of the T/H and CML to CMOS converter.
On-chip Test Signal Synthesizer

Figure 21.7.4: Test-signal synthesizer with narrow-band power amplifier.
## Performance Summary of Two Papers

<table>
<thead>
<tr>
<th>Paper 1</th>
<th>Paper 2</th>
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<tbody>
<tr>
<td><strong>Resolution</strong></td>
<td>Resolution</td>
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<tr>
<td>6b</td>
<td>6 bits</td>
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<tr>
<td><strong>Conversion rate</strong></td>
<td>Conversion rate</td>
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<tr>
<td>0.1 - 24GS/s</td>
<td>0.1 – 40 GS/s</td>
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<tr>
<td><strong>Input range</strong></td>
<td>Input range</td>
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<tr>
<td>1.2V$_{pp}$-diff</td>
<td>1.2 V$_{p-p}$ diff.</td>
</tr>
<tr>
<td><strong>ENOB</strong></td>
<td><strong>ENOB</strong></td>
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<tr>
<td>average cal / cal each freq</td>
<td>1-point cal / cal each freq</td>
</tr>
<tr>
<td>4.2/4.8, $F_{in}$ = 8GHz</td>
<td>4.5 b, $F_{in}$ = 10 GHz</td>
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<tr>
<td>3.5/4.1, $F_{in}$ = 12GHz</td>
<td>3.9 b, $F_{in}$ = 18 GHz</td>
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<tr>
<td><strong>SFDR</strong></td>
<td><strong>SFDR</strong></td>
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<tr>
<td>40dB @ 8GHz</td>
<td>40 dBc @ 10 GHz</td>
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<tr>
<td>35dB @ 12GHz</td>
<td>35 dBc @ 18 GHz</td>
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<tr>
<td><strong>Power</strong></td>
<td><strong>Power</strong></td>
</tr>
<tr>
<td>1.2W @ 1V and 2.5V</td>
<td>$\leq$ 1.5 W</td>
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<td><strong>ADC core</strong></td>
<td><strong>ADC core</strong></td>
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<td>4 x 4 mm$^2$</td>
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THANK YOU!