

FPGA Forum 2007: 24th October, Trondheim



Accurate Delay Test of FPGA Routing Network by Branched Test Paths

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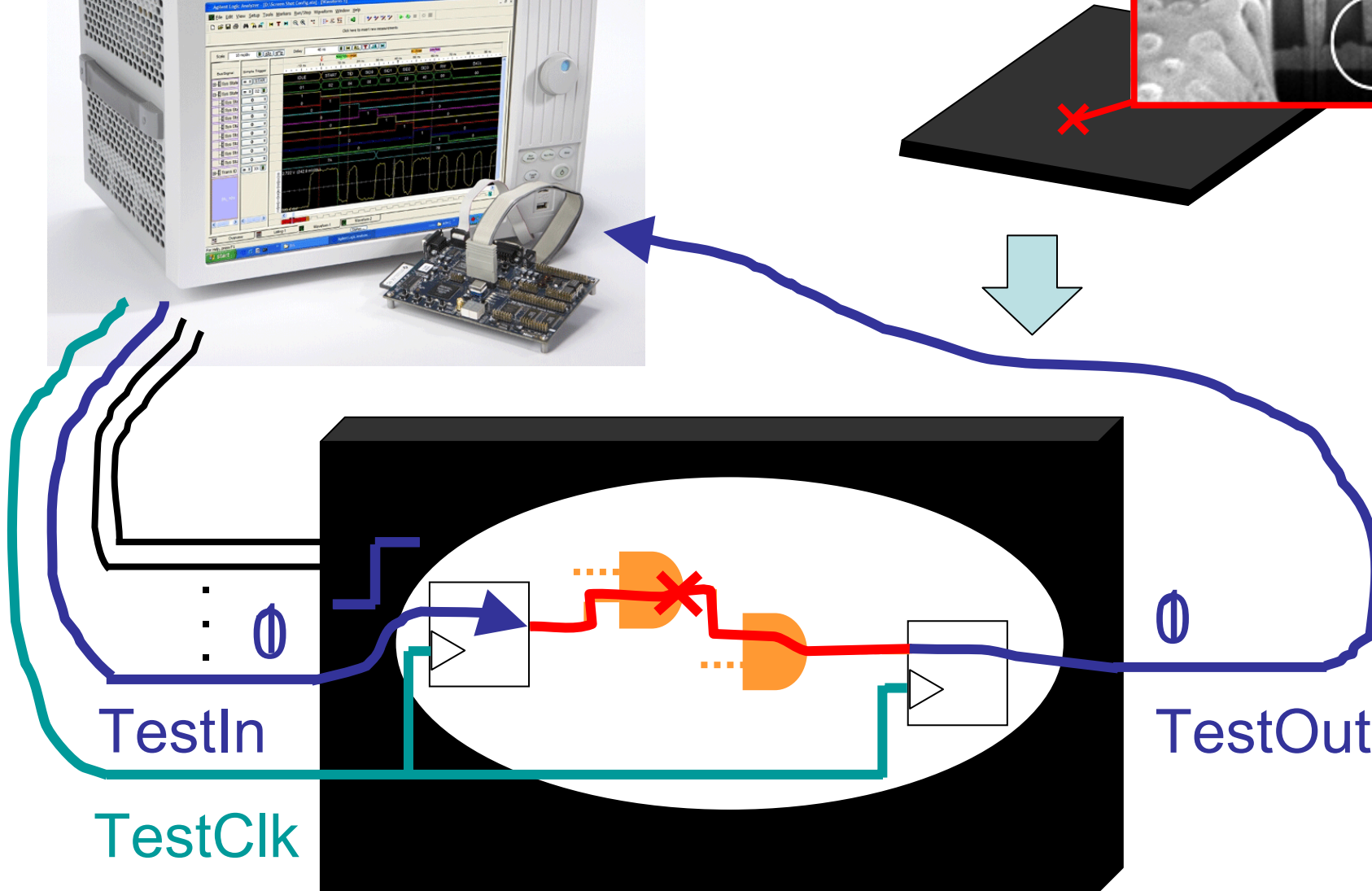
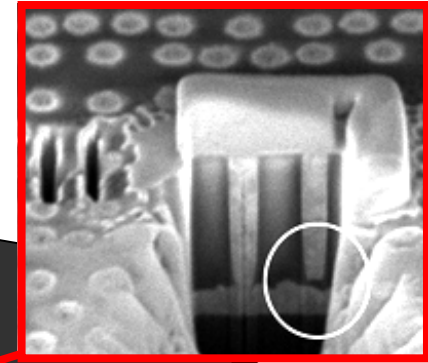
Outline

- Motivation
- Objective
- Definition of detection accuracy
- Previous work on accurate delay test
- Characterization of test paths in SPICE
- Proposed test method
- Comparison to previous work
- Conclusion

Motivation

- Number of defects increase exponentially when defect size decreases [Kruseman, ITC 04]
- 58 % of customer returned parts have open defects [Needham, ITC 98]
- Delay test is superior in detecting open defects and small defects.
- Recent research shows that fan-out increases detection accuracy in the stem of a test path [Tahoori, ITC 02]

Delay Test



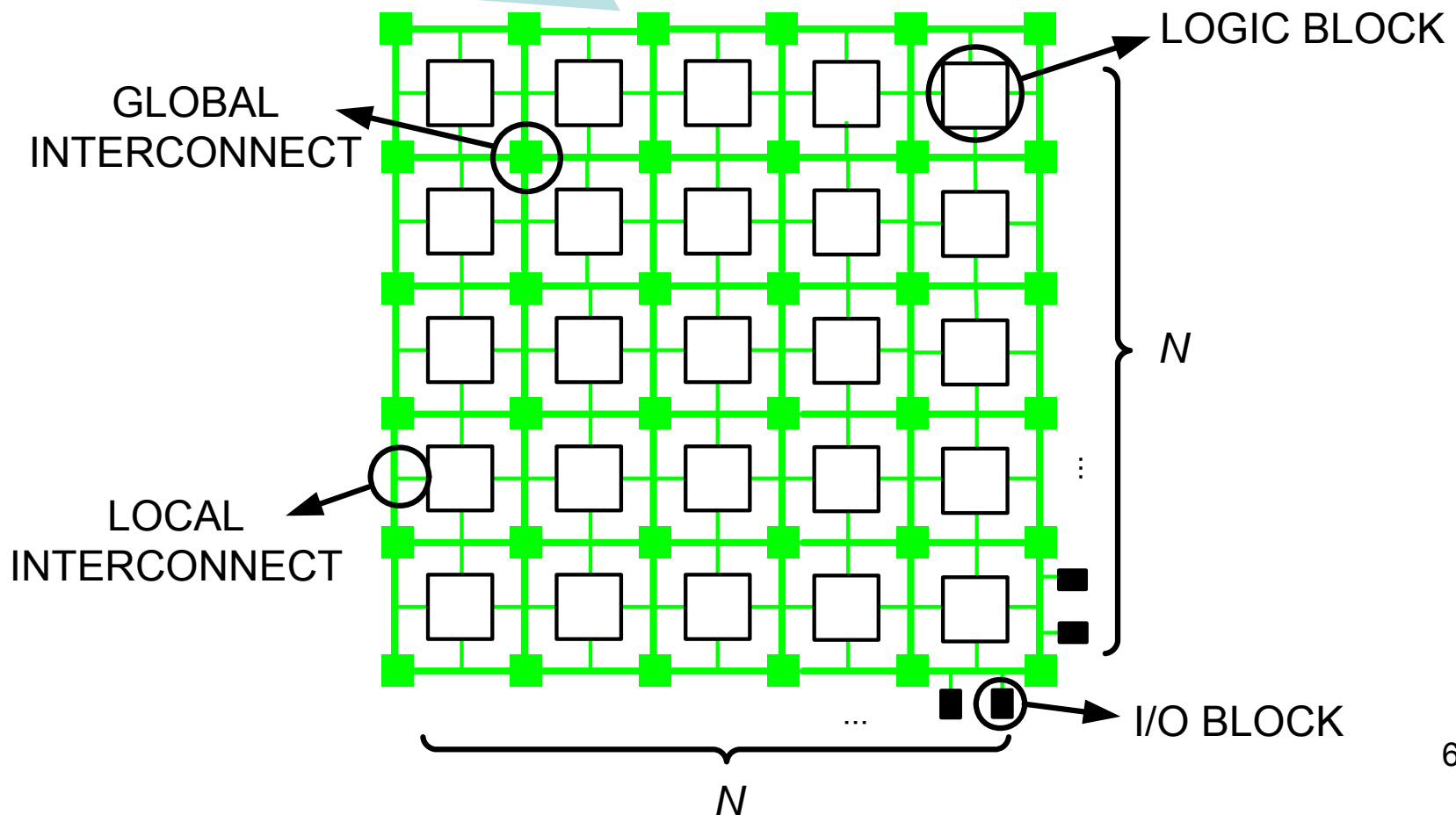
Objective

Obtain high detection accuracy of delay test in FPGA routing network

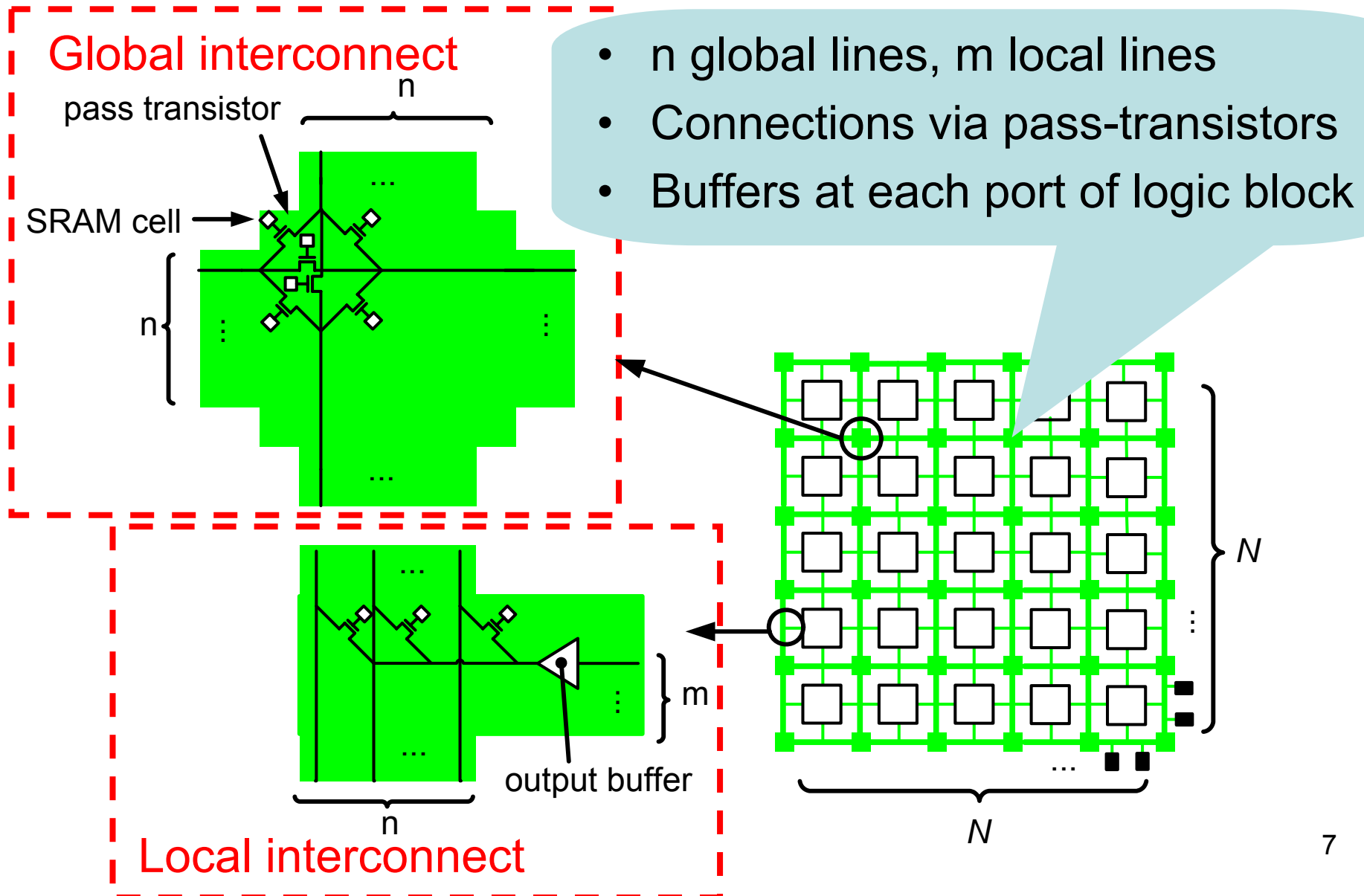
- Define detection accuracy
- Evaluate the influence of fan-out on detection accuracy (SPICE)
- Propose test configurations with short test application time
- Calculate detection accuracies for the proposed test configurations

Symmetrical island-style SRAM FPGA

- NxN symmetrical FPGA
- Islands of logic surrounded by routing resources
- Function selected by configuring SRAM memory cells



Routing network of SRAM FPGA

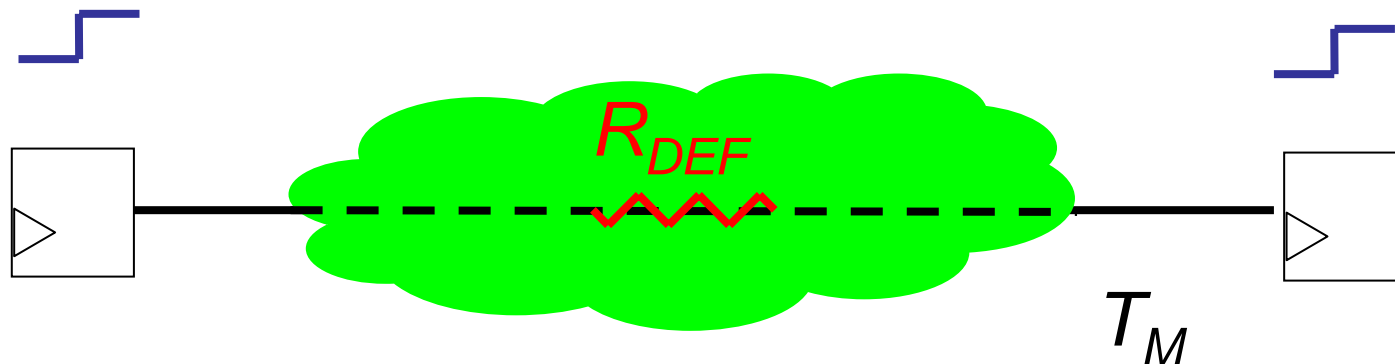


Detection accuracy

The smallest detectable defect size (R_{DEF})

$$A = \min \left\{ R_{DEF} \left| \frac{T(R_{DEF}) - T_{D0}}{T_{D0}} \geq T_M \right. \right\}$$

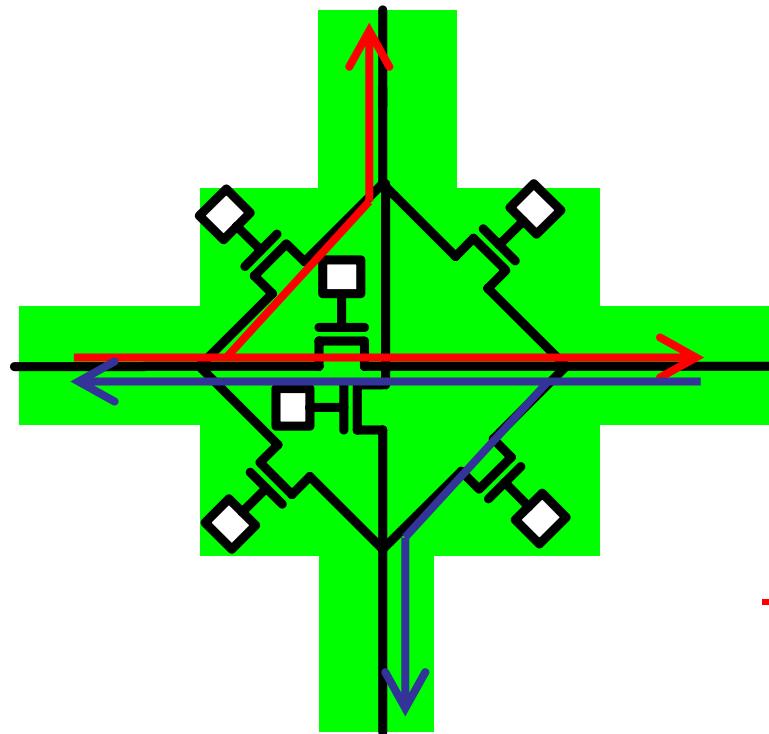
R_{DEF} : Defect resistance
 T_{D0} : delay of the fault-free path
 $T(R_{DEF})$: delay of the faulty path
 T_M : delay margin



FPGA delay test by branched test paths

[Tahoori, FPT 2002]

Detection accuracy for defects in the branches



- Unknown

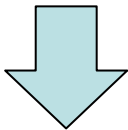
Switch matrix

Segment delay testing in FPGA

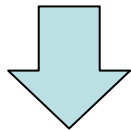
[Peng et al., DFT 2004]

Detection accuracy

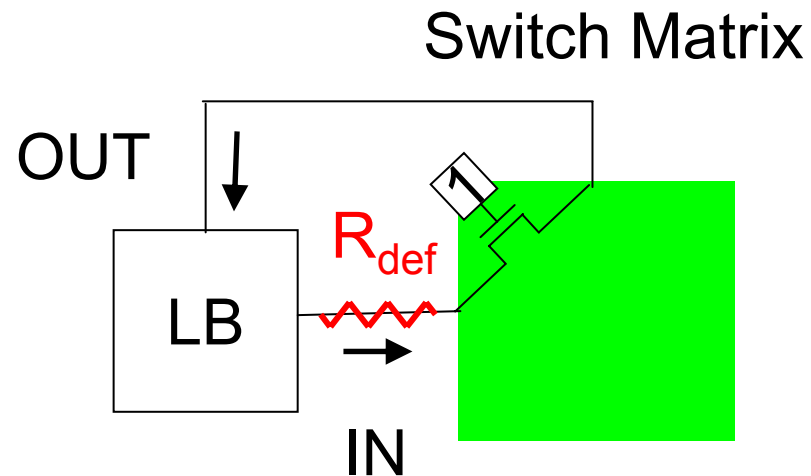
Short test path



Small delay margin



Good detection accuracy



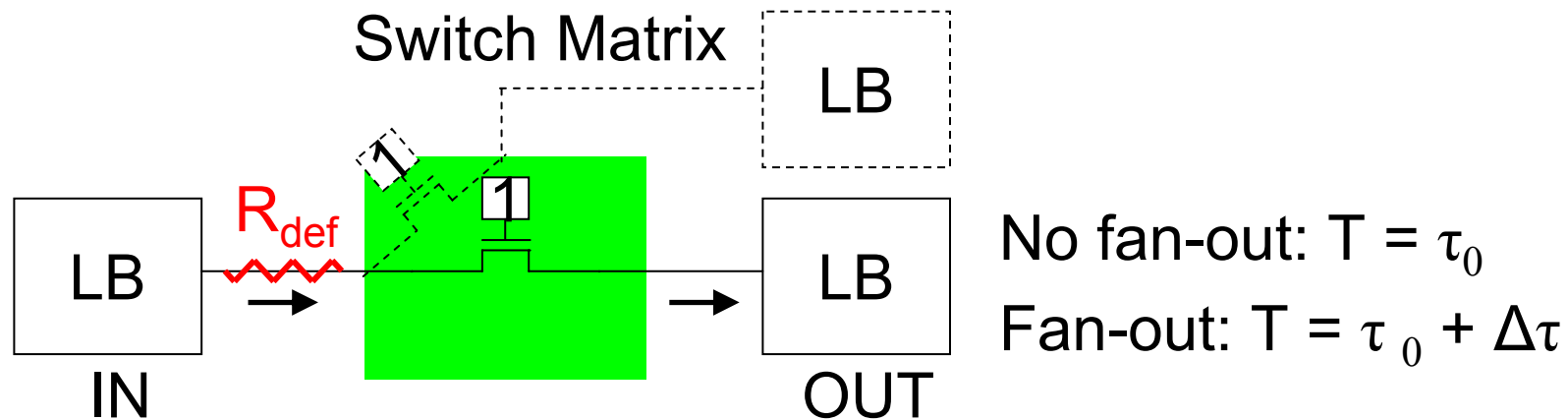
Number of test configurations

48 (XC400 like architecture)

FPGA delay test by branched test paths

[Tahoori, FPT 2002]

Detection accuracy for defects in the stem



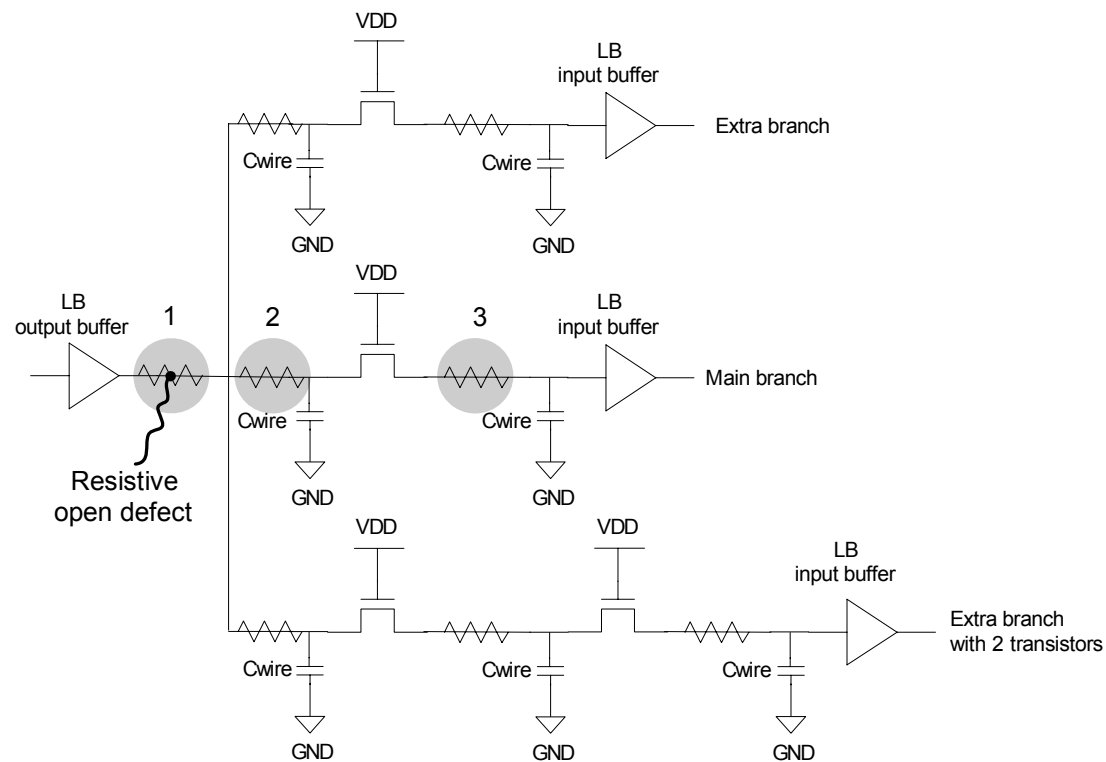
Number of test configurations

8 (Xilinx Virtex FPGA)

Measurement of detection accuracy

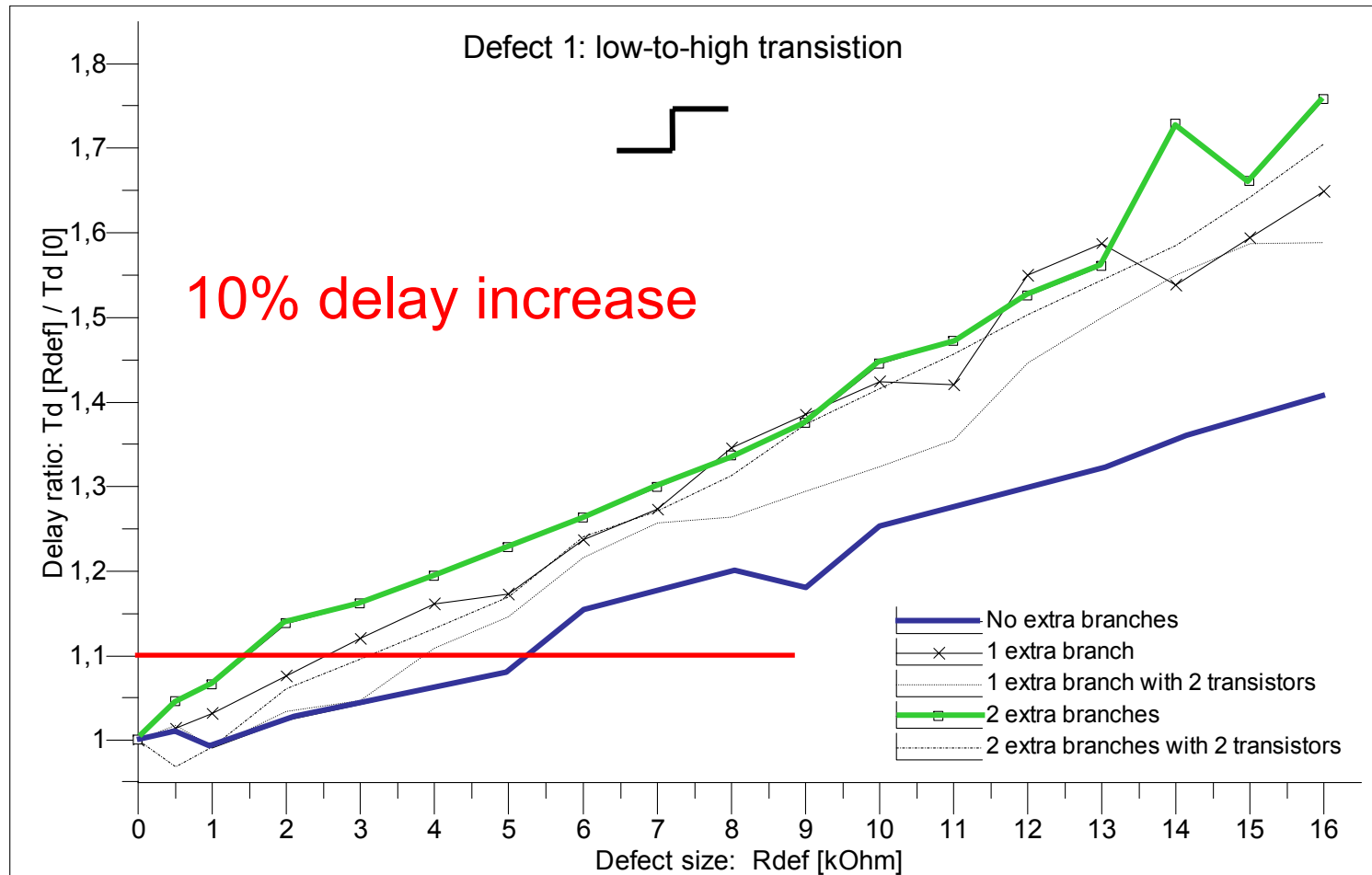
SPICE setup and defect locations:

- Tahoori's FPGA interconnect model
- 22 nm predictive transistor model
- 10 % delay margin



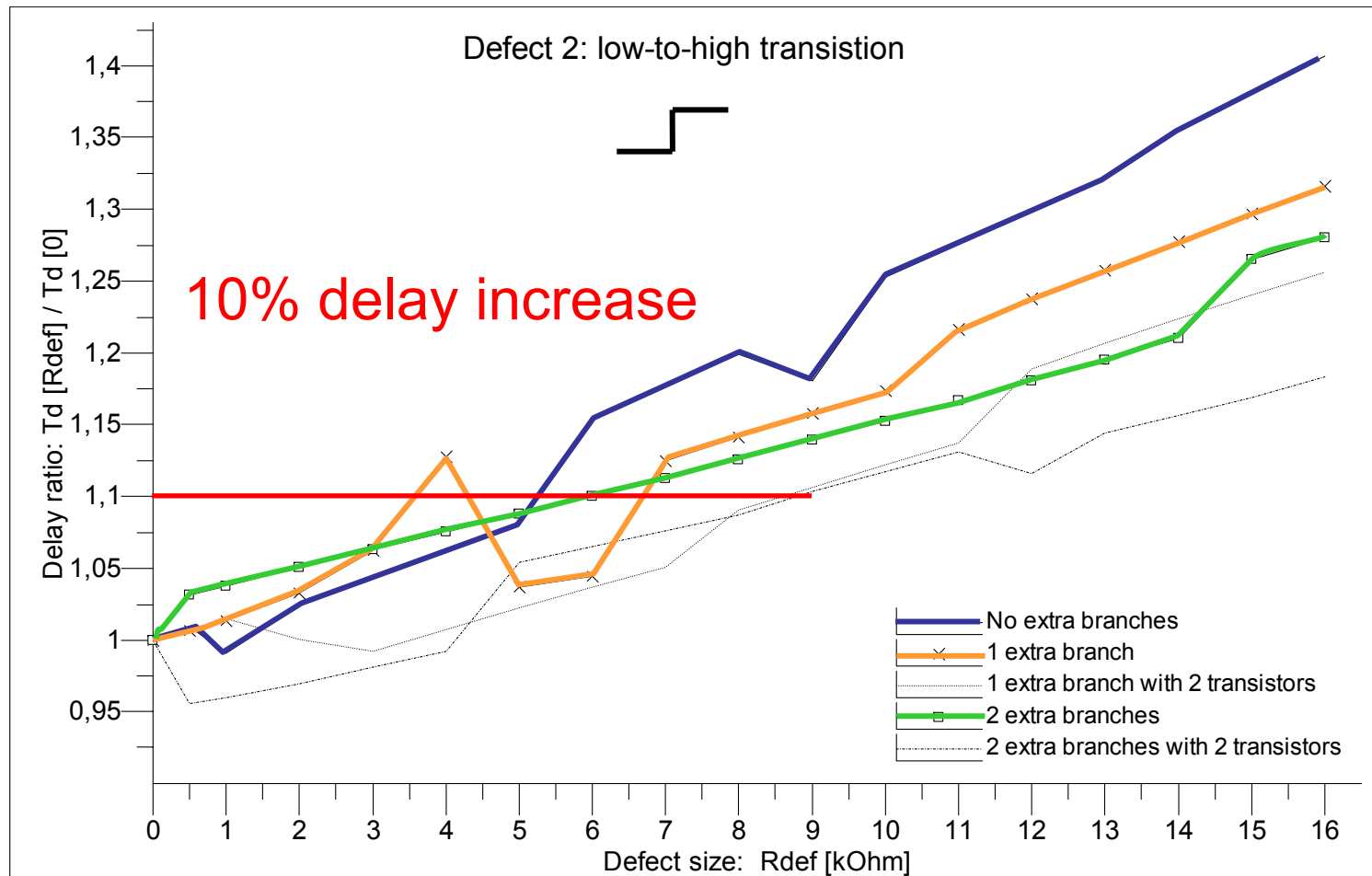
SPICE results (Defect 1)

Detection accuracy of defects in stems:



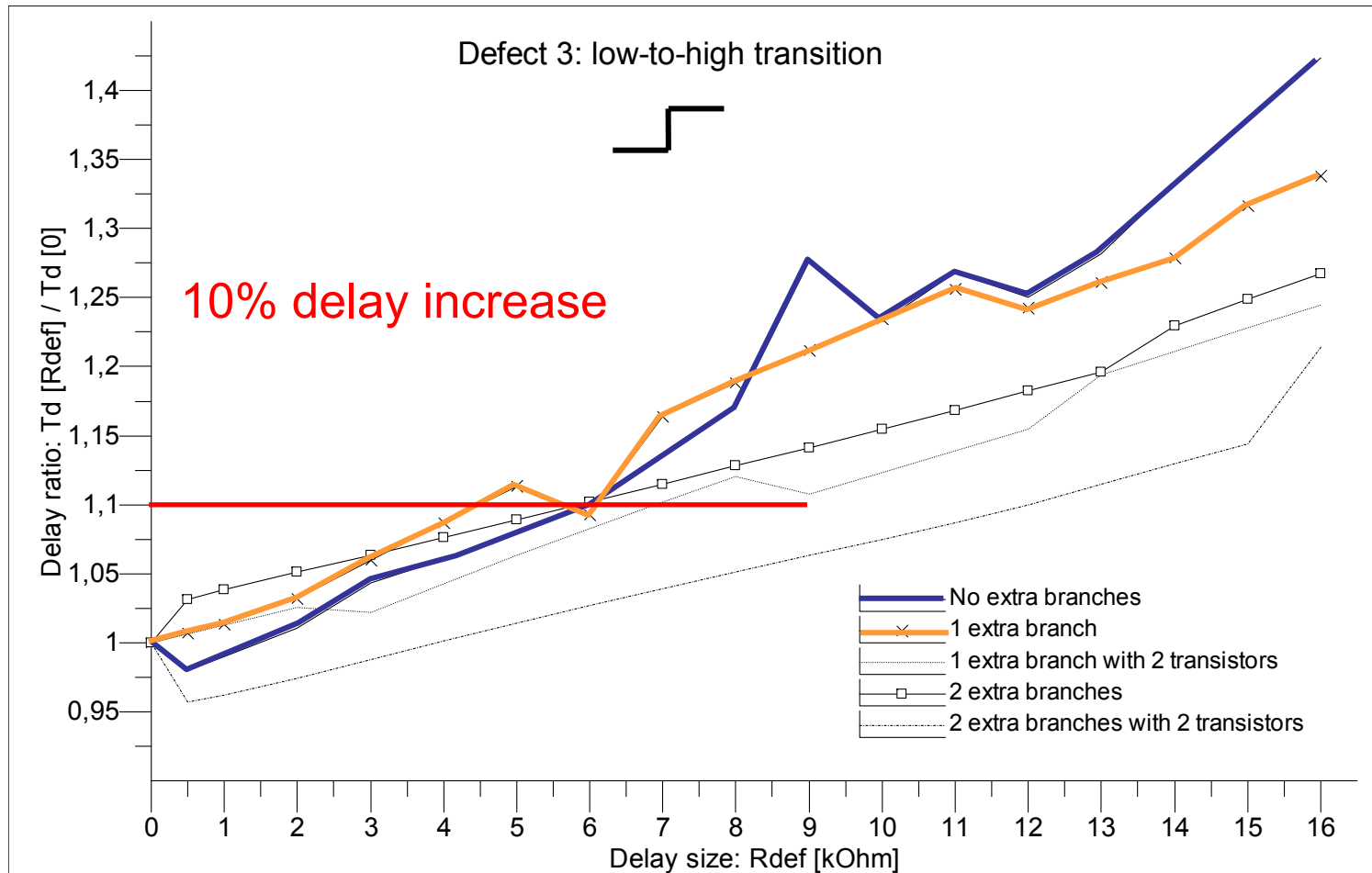
SPICE results (Defect 2)

Detection accuracy of defects in branches, close to fan-out point:



SPICE results (Defect 3)

Detection accuracy of defects in branches, far from fan-out point:



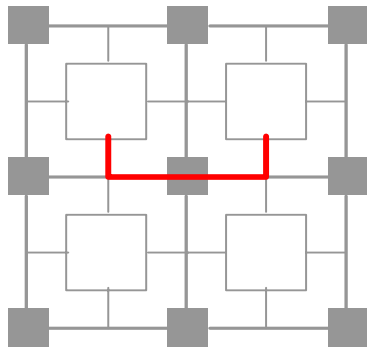
Measured detection accuracy:

Defect type	Test path type	Detection accuracy [kΩ]	
		LH	HL
Defect 1 (stem)	No fan-out	6	2
	2 branches	3	2
	3 branches	2	1
Defect 2 (fan-out point)	No fan-out	6	2
	2 branches	4	2
	3 branches	6	2
Defect 3 (branch)	No-fan-out	7	6
	2 branches	7	6
	3 branches	9	6

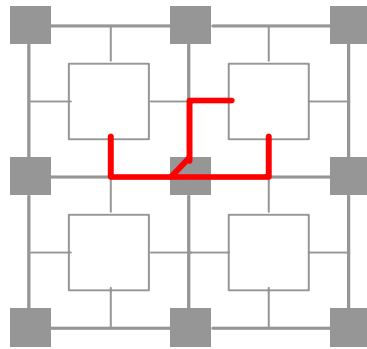
Proposed test configurations

- Use the shortest test paths

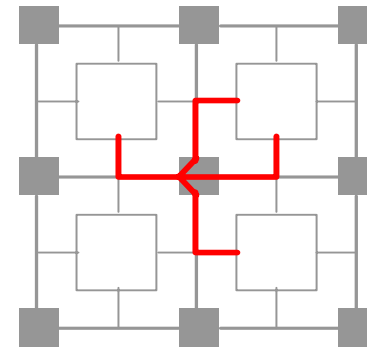
1-branch test path:



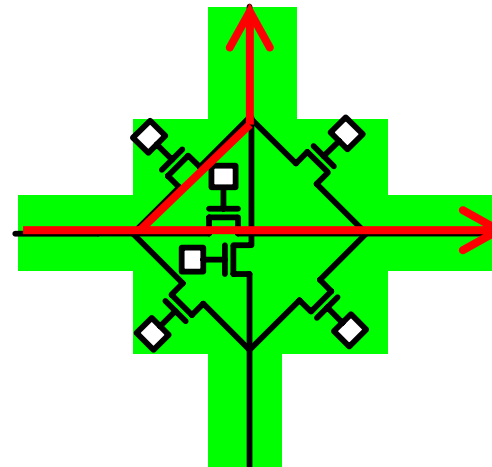
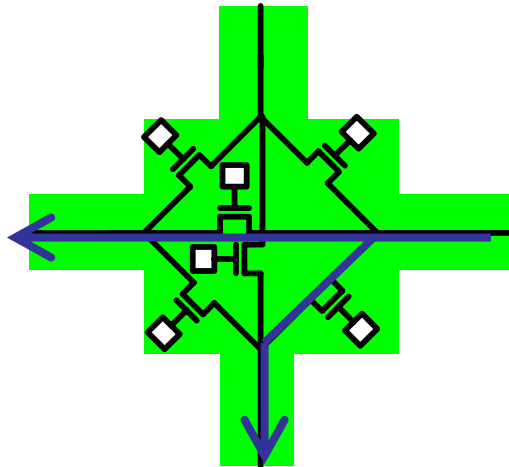
2-branch test path:



3-branch test path:

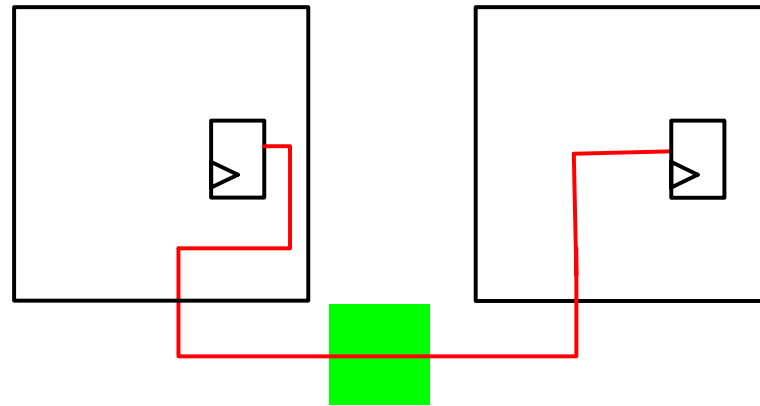


- All segments outside switch matrices tested by stems
- All segments inside switch matrices tested in both directions

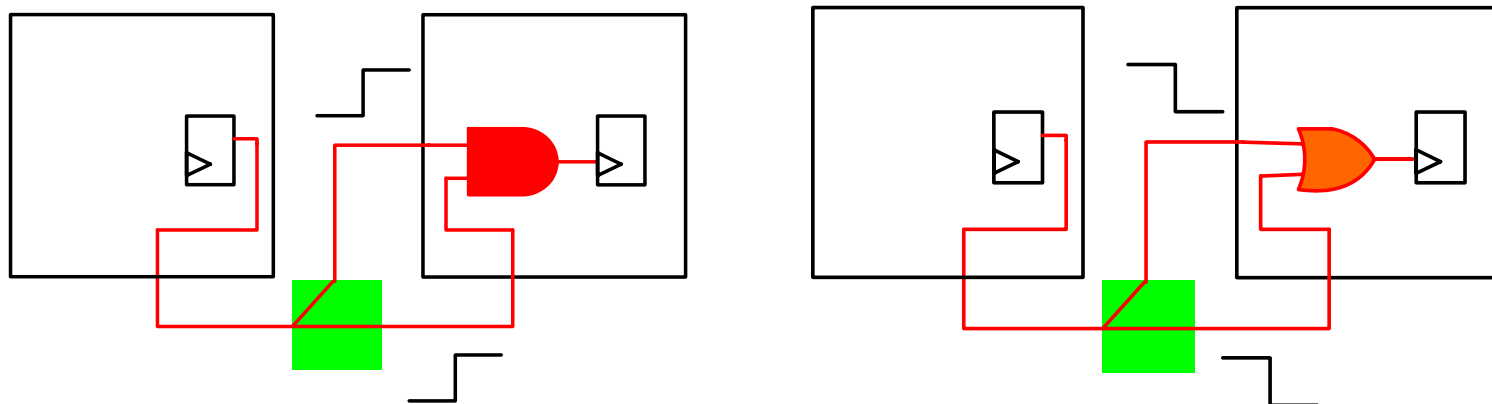


Proposed test configurations

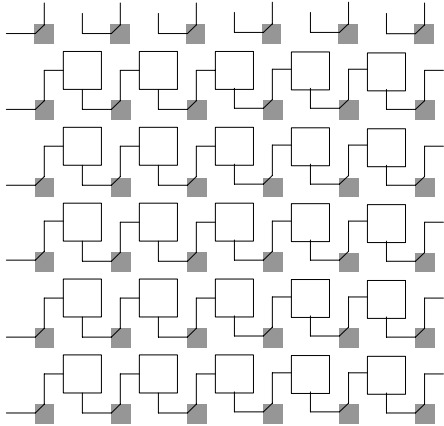
- Logic blocks with 1 input implement identity function



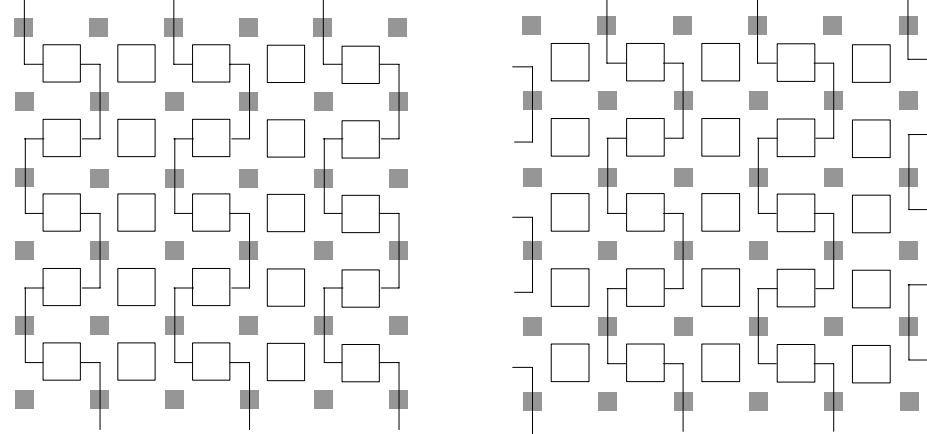
- Logic blocks with 2 inputs:
 - AND gate for rising transition delay test
 - OR gate for falling transition delay test



Test configurations, no fan-out



x 4 rotations



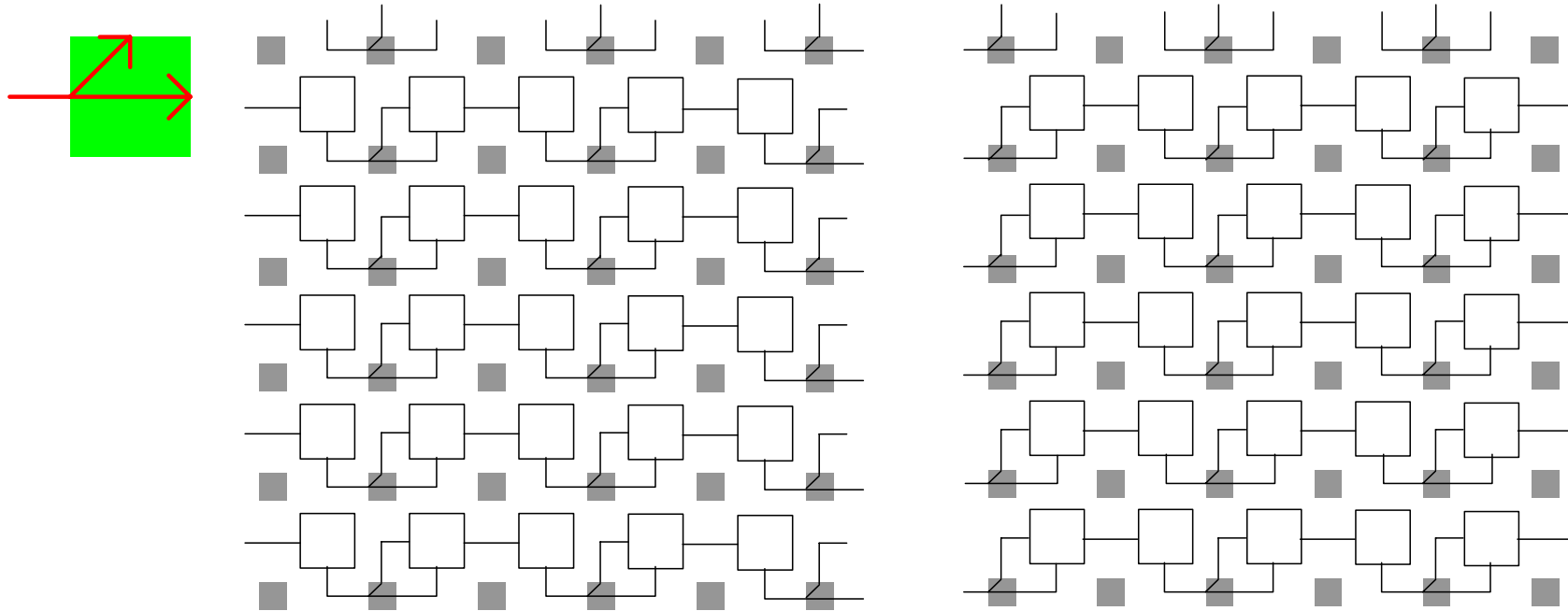
x 2 rotations

- 8 test configurations

Test procedure:

1. Reset all flip-flops
2. Apply signal transition at the primary inputs
3. Toggle test clock for N periods
4. Check at the primary outputs whether the transition has arrived

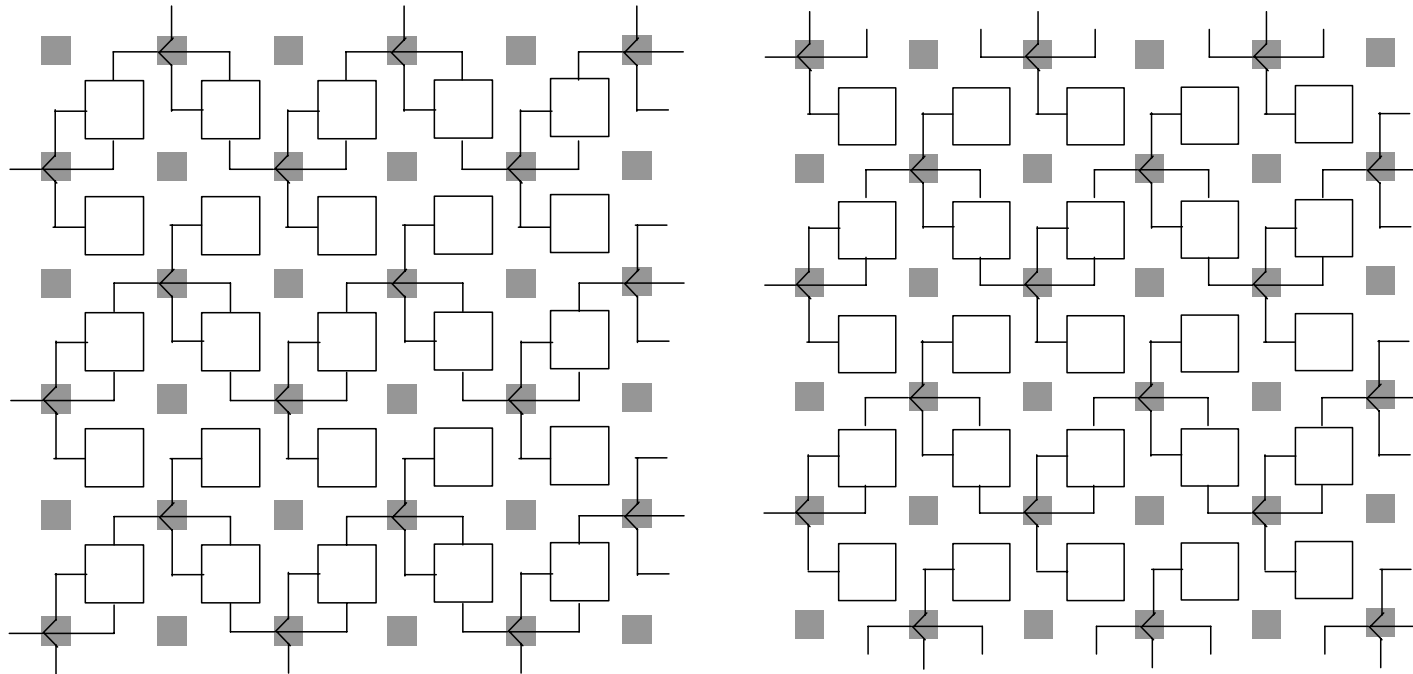
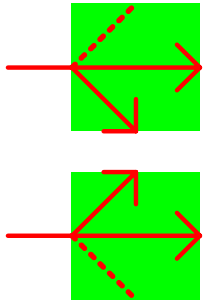
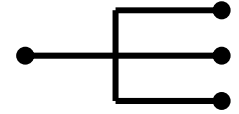
Test configurations, 2 branches



x 4 rotations x 2 mirror x (AND, OR)

- 32 test configurations

Test configurations, 3 branches

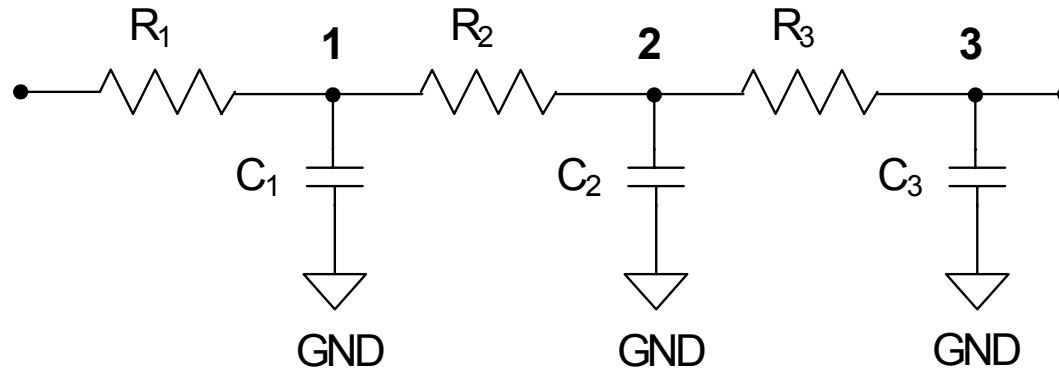


x 4 rotations x 2 mirror x (AND, OR)

- 32 test configurations

Calculated detection accuracy

1-branch test path



Elmore delay:

$$\tau = \sum_{k=1}^N C_k \sum_{m=1}^k R_m$$

$$\tau_1 = 6RC$$

Detection accuracy:

$$A_1 = \min \left\{ R_{DEF} \left| \frac{\tau(R_{DEF}) - \tau_1}{\tau_1} \geq T_M \right. \right\}$$

$$A_1 = \frac{0,6R}{x}, \text{ where } x = \begin{cases} 3 & \text{for defect 1} \\ 2 & \text{for defect 2} \\ 1 & \text{for defect 3} \end{cases}$$

Calculated detection accuracy

2-branch test path

Elmore delay

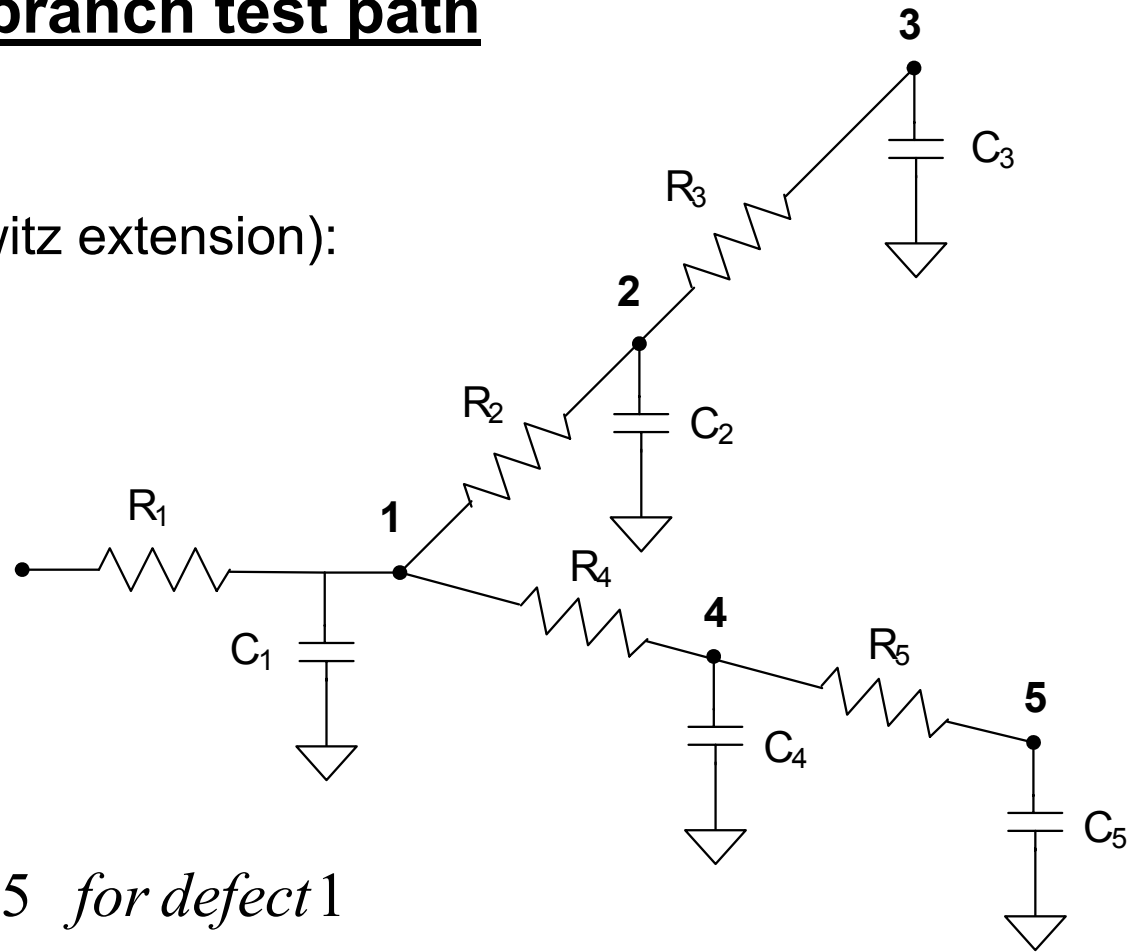
(Penfield-Rubinstein-Horowitz extension):

$$\tau_i = \sum_{k=1}^N C_k V_k(0) R_{i,k}$$

$$\underline{\tau_2 = 8RC}$$

Detection accuracy:

$$A_2 = \frac{0,8R}{x}, \text{ where } x = \begin{cases} 5 & \text{for defect 1} \\ 2 & \text{for defect 2} \\ 1 & \text{for defect 3} \end{cases}$$



Calculated detection accuracy

3-branch test path

Elmore delay

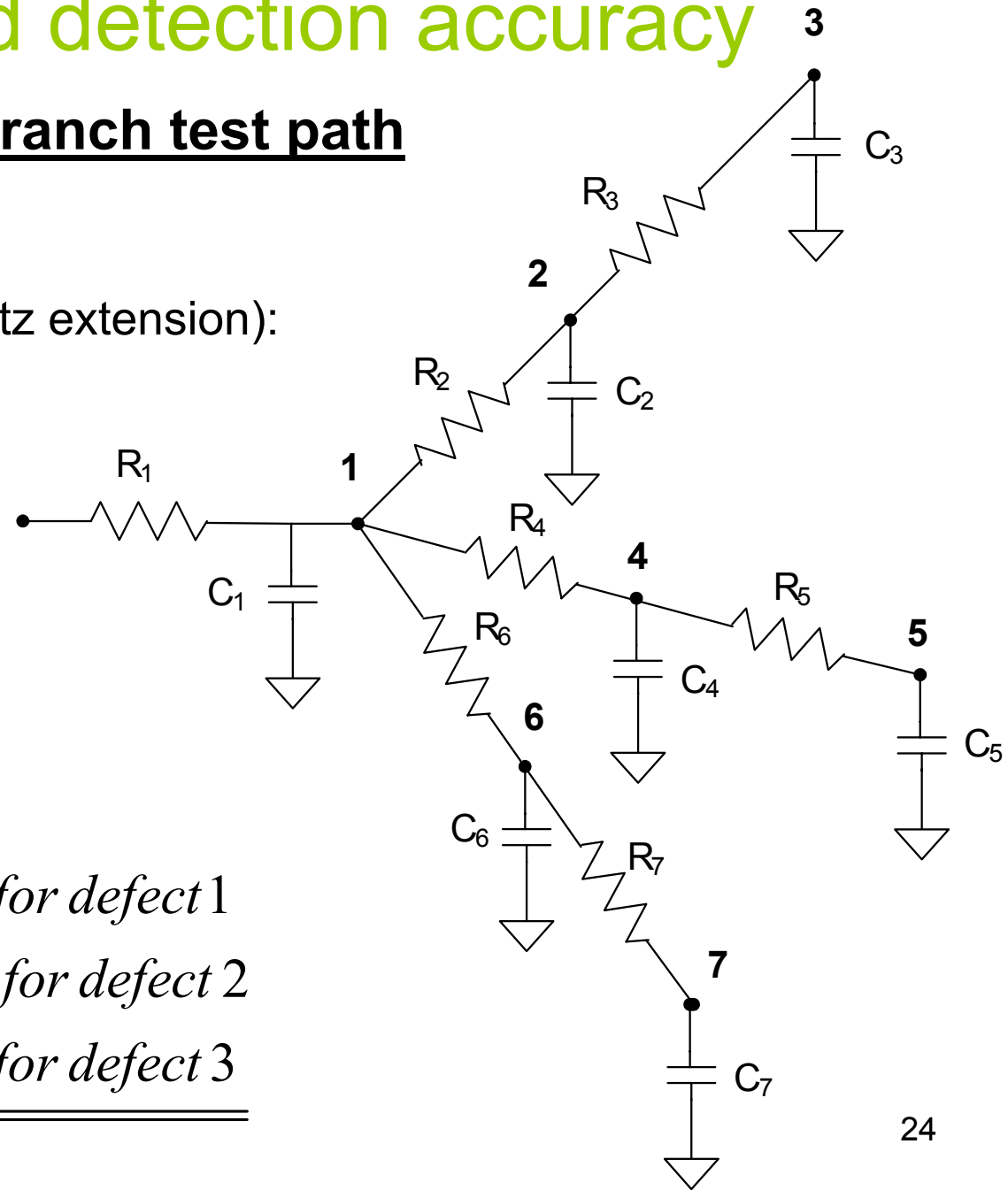
(Penfield-Rubinstein-Horowitz extension):

$$\tau_i = \sum_{k=1}^N C_k V_k(0) R_{i,k}$$

$$\underline{\underline{\tau_2 = 10RC}}$$

Detection accuracy:

$$\underline{\underline{A_2 = \frac{R}{x}, \text{ where } x = \begin{cases} 7 & \text{for defect 1} \\ 2 & \text{for defect 2} \\ 1 & \text{for defect 3} \end{cases}}}$$

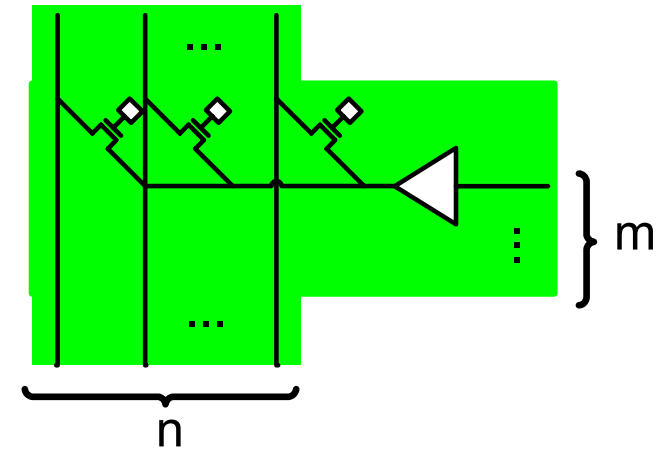


Characteristics of proposed test

- 100% segment delay fault coverage

Number of test configurations

Test path type	Defect 1 (stem)
1 branch	$8 \frac{\lceil n \rceil}{m}$
2 branches	$32 \frac{\lceil n \rceil}{m}$
3 branches	



Detection accuracy per Ω resistance

Test path type	Defect 1 (stem)	Defect 2 (f.o.p)	Defect 3 (branch)
1 branch	0,2000	0,3000	0,6000
2 branches	0,1600	0,4000	0,8000
3 branches	0,1429	0,5000	1,0000

Comparison to previous work

Proposed method / Peng's (2004) method:

Detection accuracy per Ω resistance

Test path type	Defect 1(stem)		Defect 2(f.o.p)		Defect 3 (branch)*	
	A	$(A_0 - A)/A_0$	A	$(A_0 - A)/A_0$	A	$(A_0 - A)/A_0$
1 branch	0,2000	0 %	0,3000	0 %	0,6000	66,7%

A - proposed method

A_0 - Peng's method

Number of test configurations

Test path type	Proposed method	Peng's method
1 branch	48	48

*8 % of all segments in the routing network

Comparison to previous work

Proposed method / Tahoori's (2002) method:

Detection accuracy per Ω resistance

Test path	Defect 1(stem)		
	A_0	A	$(A_0 - A) / A_0$
1branch	0,3000	0,2000	33,3 %
2 branches	0,4000	0,1600	60,0 %
3 branches	0,4833	0,1429	70,4 %

A: proposed method
 A_0 : Tahoori's method

Test path type	Defect 2(fan-out point)			Defect 3 (branch)		
	A_0	A	$(A_0 - A) / A_0$	A_0	A	$(A_0 - A) / A_0$
1 branch	0,7200	0,3000	58,3 %	3,600	0,6000	83,3 %
2 branches	0,9600	0,4000	58,3 %	4,800	0,8000	83,3 %
3 branches	1,1600	0,5000	56,8 %	5,800	5,800	82,8 %

Comparison to previous work

Proposed method / Tahoori's (2002) method:

Number of test configurations

Test path type	Proposed method	Tahoori's method
1 branch	8	8
2 branches	32	8
3 branches	32	8

Conclusions and further work

Conclusions:

- Bidirectional test boosts test accuracy by 50 %
- Accuracy in branches decreases when more branches are added

Further work:

- Study fan-out in local connections

**THANK YOU FOR YOUR
ATTENTION!**