

CURRICULUM VITAE

Short biography

Per Gunnar Kjeldsberg was born in Trondheim, Norway in 1966. He received his Sivilingeniør degree (MSc) in electrical engineering in 1992 from the Norwegian Institute of Technology. In 2001 he received the degree of Doktor ingeniør (PhD) from the same institution (now Norwegian University of Science and Technology, NTNU). Between 1992 and 1996 he worked as a design engineer at Eidsvoll Electronics, designing communication control equipment based on embedded hw/sw solutions. During his doctoral studies, he focused on storage requirement estimation and optimization for data intensive applications. The research was performed in close cooperation with IMEC, in Leuven, Belgium, where he was a visiting researcher for nine months in all. Kjeldsberg has published a number of conference and journal papers, and has been coauthor of a book in his field of interest. Currently he is Professor at Department of Electronics and Telecommunications, NTNU. His research interests are embedded hw/sw systems, with a focus on multi-media and digital signal processing applications. Between October 2005 and June 2006, Kjeldsberg was a visiting researcher at University of California, Irvine, Center for Embedded Computer Systems. At NTNU he teaches several extensive undergraduate and graduate courses, and supervises a number of students at master and PhD level. Kjeldsberg is and has been a member of the board of directors both at the Faculty and in private companies. He is frequently used as reviewer for several international journals and conferences.

Personal Information

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Date of birth: July 4, 1966, in Trondheim, Norway

Formal Education

1996-2001: Doktor Ingeniør (Ph.D., electrical engineering) from the Norwegian University of Science and Technology

1987-1992: Sivilingeniør (graduate degree in electrical engineering, microelectronics) from the Norwegian Institute of Technology (now part of NTNU)

Employment

- 2007 – Present Professor at Department of Electronics and Telecommunications, NTNU
- 2002 – 2007 Associate Professor at Department of Physical Electronics / Department of Electronics and Telecommunications, NTNU
- 2001: Associate Professor / Post.doc at Department of Physical Electronics, NTNU
- 1992-1996: Design Engineer at Eidsvoll Electronics AS
- 1988, 89, 91: Summer employment at Telenor Research and Development
- 1985-1987: Norwegian Army, trained to be and practicing as a sergeant

Current Projects and Responsibilities

- EMECS, European Master Embedded Computing Systems, an Erasmus Mundus Master Program sponsored by the European Union (EU). A cooperation between NTNU (departments at the IME faculty), University of Kaiserslautern, Germany, and University of Southampton, United Kingdom. I am deputy leader for the activities at NTNU.
- CROPS, CRoss-layer OPtimization in Short-range wireless sensor networks, a Nordic research project with six PhD students. I am co-supervisor for one PhD student.
- Teaching TFE4105 Digitalteknikk og datamaskiner, a second year course in digital design.
- Teaching TFE4140 Modelling og analyse av digitale kretser, a third year course on modeling and analysis of digital systems.
- Teaching TFE02 HW/SW Codesign med innvedde systemer, a fifth year course in HW/SW Codesign and embedded systems.
- Teaching FE8109 Design og utnyttelse av minnehierarkier i multimedia applikasjoner, a PhD student course in Design and Utilization of Memory Hierarchies in Multi-Media Applications.
- Supervising a number of students at master and PhD level.
- Member of the Board for Research and Education of Researchers at the IME-Faculty.
- Secretary and administrator of Mikroelektronikkforum, a department – industry contact group in the field of microelectronics.
- Member of the board of directors at Thelma AS since 2000 (chairman between 2001 and 2009).
- Reviewer for several academic journals and conferences in my field of interest.

Former Projects and Responsibilities

- Cuban, Co-optimized Ubiquitous Broadband Access Networks, a Norwegian Research Council project in cooperation with five other professors and associate professors at our department. Eight PhD candidates were educated within this project. I supervised two of them.
- EMBLA, a Norwegian Research Council project focusing on EMBedded systems design, modeling, Languages and Analysis (2003-2005). It had participation from ten Norwegian industrial companies in addition to educational and research establishments.
- CoDeVer, a Norwegian Research Council project focusing on Codesign and Coverification (1999-2002). It had participation from ten industrial companies in addition to educational and research establishments.
- Commissioner for equal opportunities at the IME-Faculty (2002-2005)
- Member of the board of directors at Eidsvoll Electronics AS (1995-1999 and 2003-2007).
- Member of the IME-Faculty Board (1999).

Presentations, Training Courses, and Research Visits

- November 2009: IEEE NORCHIP Conference, Trondheim, Norway. I was member of the program committee and chair in two sessions.
- October 2008: FPGA-forum (Norwegian FPGA seminar). I was chair in one of the sessions.
- October 2005-
June 2006: Visiting researcher at Center of Embedded Computer Systems, University of California, Irvine. Invited by Prof. Nikil Dutt.
- August 2003: Swedish National Summer School on Multiprocessor Systems on Chip, Örebro, Sweden. I was invited to present a talk on "Optimized Design and Use of Memory Hierarchies in Data Intensive Multi-Media Applications".
- October 2002: DAK Forum (Norwegian CAD Seminar), Vidar A. Pettersen and I gave a presentation of tools and platforms for HW/SW Codesign.
- March 2002: Design Automation and Test in Europe, DATE 2002, Paris, France, March 2002. I presented the cad tool I developed during my Ph.D. at the University Booth.
- June 2001: 38th Design Automation Conference, DAC 2001, Las Vegas, NV, USA. I presented a paper on "Detection of Partially Simultaneously Alive Signals in Storage Requirement Estimation for Data Intensive Applications". I also presented my work in the Ph.D. Forum and at the University Booth at the conference.
- October-
December 2000: Repeated visit to IMEC in Leuven, Belgium. I continue my work with Francky Catthoor and his colleagues within the field of Data Transfer and Storage Exploration.
- November 2000: International Conference on Computer Aided Design, ICCAD 2000, San Jose, USA. I presented a paper on Automated Data Dependency Size Estimation with a Partially Fixed Execution Ordering
- June 2000: IEEE Nordic Signal Processing Symposium, NORSIG 2000, Kolmården, Sweden. I presented a paper on "Application of High-Level Memory Size Estimation for Guidance of Loop Transformations in Multimedia Design".
- May 2000: The 8th International Workshop on HW/SW Codesign, CODES 2000, San Diego, USA. I presented a paper on "Storage Requirement Estimation for Data Intensive Applications with Partially Fixed Execution Ordering".
- October 1999: DAK Forum (Norwegian CAD Seminar), I gave a presentation of the "Data Transfer and Storage Exploration" from IMEC.
- September 1999: How to write high-performance low-power multimedia application code, IMEC, Belgium
- January-July
1999: Visiting IMEC in Leuven, Belgium. I worked with Francky Catthoor and his colleagues within the field of Data Transfer and Storage Exploration
- January 1999: C++ based Hardware Design of Complex Digital Systems, IMEC, Belgium

- October 1998: DAK Forum (Norwegian CAD Seminar), I gave a presentation of codesign methodologies, emphasizing topics that are presently important in the research community.
- August 1998: NATO Advanced Study Institute course in System Level Synthesis, Il Ciocco, Italy.
- June 1998: ARM Microprocessor Training Seminar, Stansted, England
- October 1996: Hardware/Software Codesign Advanced Course, Grenoble, France
- October 1995: DAK Forum (Norwegian CAD Seminar), I presented Eidsvoll Electronics' experience going from UNIX to Windows NT as CAD OS.

Publications

Journal Papers

- Kjeldsberg, P.G., Catthoor, F., Verdoolaege, S., Palkovic, M., Vandecappelle, A., Hu, Q., and Aas, E.J., "Guidance of Loop Ordering for Reduced Memory Usage in Signal Processing Applications", Springer Journal of Signal Processing Systems Vol. 53, No. 3, December 2008, pp. 301 - 321.
- Balasa, F., Kjeldsberg, P.G., Palkovic, M., Vandecappelle, A., Hu, Q., Zhu, H., and Catthoor, F., "Storage Estimation and Design Space Exploration Methodologies for the Memory Management of Signal Processing Applications", Springer Journal of Signal Processing Systems, Vol. 53, No. 1-2, pp. 51 - 71. Invited submission after ASAP 2006 conference.
- Hu, Q., Kjeldsberg, P.G., Vandecappelle, A., Palkovic, M., and Catthoor, F., "Incremental Hierarchical Memory Size Estimation for Steering of Loop Transformations", ACM Transactions on Design Automation of Electronic Systems, Vol. 12, No. 4, September 2007, pp. 50 - 50:27.
- Thörnberg, B., Palkovic, M., Hu, Q., Olsson, L., Kjeldsberg, P.G., O'Nils, M., and Catthoor, F., "Bit-Width Constrained Memory Hierarchy Optimization for Real-Time Video Systems", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 26, No. 4, April 2007, pp. 781 – 800.
- Dybdahl, H., Kjeldsberg, P.G., Grannæs, M., and Natvig, L., "Destructive-Read in Embedded DRAM, Impact on Power Consumption", Journal of Embedded Computing, IOS Press, Vol. 2, No. 2, 2006, pp. 249 - 260.
- Thörnberg, B., Hu, Q., Palkovic, M., O'Nils, M., and Kjeldsberg, P.G., "Polyhedral space generation and memory estimation from interface and memory models of real-time video systems", Elsevier Journal of Systems and Software, Vol. 79, No 2, February 2006, 231-245.
- Kjeldsberg, P.G., Catthoor, F., and Aas, E.J., "Storage Requirement Estimation for Optimized Design of Data Intensive Applications", ACM Transactions on Design Automation of Electronic Systems, Vol. 9, No. 2, April 2004, pp. 133-158.
- Kjeldsberg, P.G., Catthoor, F., and Aas, E.J., "Data Dependency Size Estimation for use in Memory Optimization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 22, No. 7, July 2003, pp. 908-921.
- Panda, P.R., Catthoor, F., Dutt, N.D., Danckaert, K., Brockmeyer, E., Kulkarni, C., Vandercappelle, A., and Kjeldsberg, P.G. "Data and memory optimization techniques for embedded systems", ACM Transactions on Design Automation of Electronic Systems, Vol. 6, No 2, April 2001, pp. 149 - 206 (the most downloaded article from ACM TODAES (568 times) between July 02, 2008 and 2009).

Conference Papers

- Yassin, Y.H., Kjeldsberg, P.G., Hulzink, J., Romero, I., and Huisken, J., "Ultra Low Power Application Specific Instruction-Set Processor Design for a Cardiac Beat Detector Algorithm", IEEE NORCHIP Conference, NORCHIP 2009, Trondheim, Norway, November 2009.
- Miniskar, N.R., Hammari, E., Munaga, S., Mamagkakis, S., Kjeldsberg, P.G., and Catthoor, F., "Scenario Based Mapping of Dynamic Applications on MPSoC: A 3D Graphics Case Study", accepted for publication at The International Symposium on Systems, Architectures, MOdeling and Simulation (SAMOS IX), July 2009, Samos, Greece.
- Havashki, A., Lundheim, L., Kjeldsberg, P.G., Gustafsson, O., and Øien, G.E., "Analysis of switching activity in DSP signals in the presence of noise", accepted for publication at The IEEE Region 8 EUROCON 2009 Conference, May 2009, St. Petersburg, Russia.
- Havashki, A., Lundheim, L., Kjeldsberg, P.G., and Øien, G.E., "Effects of Finite Coefficient Word Length on Channel Estimator Performance", IEEE International Conference on Signal Processing, ICSP2008, Beijing, China, October 2008, pp. 402 - 405.
- Oskuii, S.T., Kjeldsberg, P.G., Lundheim, L., and Havashki, A., "Power Optimization of Parallel Multipliers in Systems with Variable Word-length", International Workshop on Power And Timing Modeling, Optimization and Simulation, PATMOS 2008, Lisbon, Portugal, September 2008. Published in Springer Lecture Notes in Computer Science, Vol. 5349, January 2009, pp. 103 - 115.
- Oskuii, S.T., Johansson, K., Gustafsson, O., and Kjeldsberg, P.G., "Power Optimization of Weighted Bit-Product Summation Tree for Elementary Function Generator", IEEE International Symposium on Circuits and Systems, ISCAS 2008, Seattle, USA, May 2008, pp. 1240 - 1243.
- Oskuii, S.T., Kjeldsberg, P.G., and Gustafsson, O., "Power Optimized Partial Product Reduction Interconnect Ordering in Parallel Multipliers", IEEE NORCHIP Conference, NORCHIP 2007, Aalborg, Denmark, November 2007.
- Havashki, A., Kjeldsberg, P.G., Øien, G.E., Lundheim, L., and Nymoen, J.T., "On the impact of fixed point DSP implementation on required channel estimator complexity in communication receivers", IEEE International Symposium on Wireless Communication Systems, ISWCS 2007, Trondheim, Norway, October 2007, pp. 469 - 474.
- Gustafsson, O., Oskuii, S.T., Johansson, K., and Kjeldsberg, P.G., "Low-Power Realization of FIR Filters with Correlated Input Data on MAC-Based Architectures", International Workshop on Power And Timing Modeling, Optimization and Simulation, PATMOS 2007, Gothenburg, Sweden, September 2007. Printed in Lecture Notes in Computer Science, Vol 4644/2007, pp. 526-535, Springer.
- Hu, Q., Vandecappelle, A., Kjeldsberg, P.G., Catthoor, F., and Palkovic, M., "Fast Memory Footprint Estimation based on Dependency Distance Vector Calculation", Design, Automation and Test in Europe, DATE 2007, Nice, France, April 2007, pp. 379-384.
- Oskuii, S.T., Kjeldsberg, P.G., and Gustafsson, O., "Transition-activity Aware Design of Reduction-stages for Parallel Multipliers", ACM Great Lake Symposium on VLSI, GLSVLSI 2007, Stresa - Lago Maggiore, Italy, March 2007, pp. 120-125.
- Oskuii, S.T., Kjeldsberg, P.G., and Aas, E.J., "Probabilistic Gate-level Power Estimation using a Novel Waveform Set Method", ACM Great Lake Symposium on VLSI, GLSVLSI 2007, Stresa - Lago Maggiore, Italy, March 2007, pp. 37-42.
- Balasa, F., Kjeldsberg, P.G., Palkovic, M., Vandecappelle, A., and Catthoor, F., "Loop Transformation Methodologies for Array-Oriented Memory Management", invited paper at IEEE 17th International Conference on Application-specific Systems, Architectures and Processors, ASAP 2006, Steamboat Springs, Colorado, USA, September 2006.
- Hu, Q., Vandecappelle, A., Palkovic, M., Kjeldsberg, P.G., Brockmeyer, E., and Catthoor, F., "Hierarchical Memory Size Estimation for Loop Fusion and Loop Shifting of Data Dominated Applications", 11th Asia and South Pacific Design Automation Conference, ASP-DAC 2006, Yokohama City, Japan, January 2006, pp. 606-611.
- Hu, Q., Brockmeyer, E., Palkovic, M., Kjeldsberg, P.G., and Catthoor, F., "Memory Hierarchy Usage Estimation for Global Loop Transformations", IEEE NORCHIP Conference, NORCHIP 2004, Oslo, Norway, November 2004, pp. 301-304.

- Hu, Q., Palkovic, M., Kjeldsberg, P.G., "Memory Requirement Optimization with Loop Fusion and Loop Shifting", 30th Euromicro conference, Rennes, France, Aug 31 - Sep 3 2004, pp. 272-278.
- Rydland, P., Palkovic, M., Kjeldsberg, P.G., Brockmeyer, E., and Catthoor, F., "Inter in-place storage size requirement estimation", IEEE NORCHIP Conference, NORCHIP 2003, Riga, Latvia, November 2003, pp. 240-243.
- Kjeldsberg, P.G., Catthoor, F., Aas, E.J., and Palkovic, M. "STOREQ: STORage REquirement Estimation and Optimization Tool for Data Intensive Applications", Design, Automation and Test in Europe, DATE 2002, Paris, France, March 2002, Designers' Forum, pp. 256.
- Kjeldsberg, P.G., Catthoor, F., and Aas, E.J. "Detection of Partially Simultaneously Alive Signals in Storage Requirement Estimation for Data Intensive Applications", 38th Design Automation Conference, DAC 2001, Las Vegas, NV, USA, June 2001, pp. 365-370.
- Kjeldsberg, P.G., Catthoor, F., and Aas, E.J. "Automated Data Dependency Size Estimation with a Partially Fixed Execution Ordering", International Conference on Computer Aided Design, ICCAD 2000, San Jose, USA, November 2000, pp. 44-50.
- Kjeldsberg, P.G., Catthoor, F., and Aas, E.J. "Application of High-Level Memory Size Estimation for Guidance of Loop Transformations in Multimedia Design", IEEE Nordic Signal Processing Symposium, NORSIG 2000, Kolmården, Sweden, June 2000, pp. 371-374.
- Kjeldsberg, P.G., Catthoor, F., and Aas, E.J. "Storage Requirement Estimation for Data Intensive Applications with Partially Fixed Execution Ordering", International Workshop on HW/SW Codesign, CODES 2000, San Diego, USA, May 2000, pp. 56-60.

Books

- Catthoor, F., Danckaert, K., Kulkarni, C., Brockmeyer, E., Kjeldsberg, P.G., Van Achteren, T., and Omnes, T., "Data Access and Storage Management for Embedded Programmable Processors", Kluwer Academic Publishers, Dordrecht, The Netherlands, 2002, ISBN 0-7923-7689-7.
- Kjeldsberg, P.G., "Storage Requirement Estimation and Optimization for Data Intensive Application", Doctoral Thesis, Norwegian University of Science and Technology, Defended March 23, 2001, ISBN 82-7984-174-1.

Miscellaneous

- Kjeldsberg, P.G., "Mikroelektronikkprisen 2008", Elektronikk, nr. 2, 2009, pp. 35 ("Microelectronics Prize 2008", published in the Norwegian magazine Elektronikk, No. 2, 2009).
- Kjeldsberg, P.G., "Suksess for FPGA-forum", Elektronikk, nr. 11, 2006, pp. 16 ("Success for FPGA-forum", published in the Norwegian magazine Elektronikk, No. 11, 2006).
- Kjeldsberg, P.G., "Mikroelektronikkprisen 2006", Elektronikk, nr. 11, 2006, pp. 18 ("Microelectronics Prize 2006", published in the Norwegian magazine Elektronikk, No. 11, 2006).
- Kjeldsberg, P.G., "STOREQ: STORage REquirement Estimation and Optimization tool for Data Intensive Applications", European Research Consortium for Informatics and Mathematics, ERCIM News, No. 52, January 200, pp. 29-30.
- Kjeldsberg, P.G., "DATE i fortsatt vekst", Elektronikk, nr. 4, 2002, 18-20 ("DATE in continued growth", published in the Norwegian magazine Elektronikk, No. 4, 2002).
- Kjeldsberg, P.G., "En introduksjon til codesign: hva, hvordan og hvorfor?", Elektronikk, nr. 12, 1998, 48-54 ("An Introduction to Codesign: What, How, and Why?", published in the Norwegian magazine Elektronikk, No. 12, 1998).

My Background and Research Interests

After finishing high school I served one and a half year in the Norwegian army. One year is obligatory in Norway, but wanting to get something useful out of my time there, I decided to be trained as a sergeant. Having finished my one-year, I continued to serve as a sergeant until the

university semester started in the fall. Already in this first semester of my master study I realized that digital design was my main interest. In the following years I specialized in microelectronics and digital design methodologies in particular. For my master thesis I made a fast compiler-based functional simulator for sequential circuits. The topic was proposed by the design company Nordic Semiconductors ASA. During summer employment at Telenor Research and Development, the national telecommunications operator's research center, I also gained more experience with design and design tools. The first two years I worked with computer backup and assistance, but the last year I worked in the Microelectronics Department with CAD tools from Mentor Graphics.

When I left the university in the spring of 1992 I went to work with Eidsvoll Electronics AS (EIDEL) as a design engineer. I worked on many different topics, varying from computer aided circuit design, laboratory prototype testing, and system installation, to discussions with customers about future products and contracts. I also had responsibilities at external training courses, teaching customers how to use our equipment. The main product of my department at EIDEL was radio remote control equipment. It was typically realized as embedded systems, with a microprocessor running software and controlling analog circuits and digital logic in Programmable Logic Devices.

In august 1996 I started working towards my doctoral degree under supervision of Professor Einar J. Aas in the Circuit and Systems group of Department of Physical Electronics, NTNU. Ever since I left the university four years earlier, I had planned to continue my studies after having gained some industrial experience. My work as a sergeant, as an amateur actor during my student days, and as a lecturer at EIDEL, had also given me practice and interest in public speaking, and in teaching. Being important parts of the duties at a university, this also encouraged me to return. I was hired on an open department grant, and consequently had quite a bit of influence on what my research topic should be. While I worked at EIDEL, I had met with the challenges of embedded systems design, experiencing the lack of tools and methodologies when designing systems encompassing both hardware and software. This was the main reason why Hardware/Software Codesign was selected as my field of research.

Most of my first two years was used taking obligatory doctoral courses, working for the department, and getting a good understanding of my subject. I was then able to start more in-depth research. My group at the university has wide experience working with low power issues, in particular for Digital Signal Processing applications. Research on circuit partitioning has also been a main concern. This local knowledge facilitated my own research in power estimation for hardware/software partitioning. In January 1999 I went for a six month research stay at IMEC in Leuven, Belgium. Here I worked with Francky Catthoor (IEEE Fellow) and his System Exploration for Memory and Power (SEMP) group. They perform research on design methodologies for embedded multimedia systems. For this class of applications, data transfer and storage is a dominating cost factor. This is the case for *chip size*, since large memories are usually needed, *performance*, since accessing the memories may very well be the main bottleneck, and *power consumption*, since the memories and buses consume large quantities of power. A Data Transfer and Storage Exploration (DTSE) methodology is being developed for high level system design. The application is described in C code, which is then step by step transformed into a more storage optimal implementation. During the stay I changed the focus of my research somewhat to be able to work closer with the people in the SEMP group. At each optimization step in the DTSE methodology, estimation of memory size is needed to guide the selection of the best solution. My work was thus concerned with storage requirement estimation: *How may we achieve a fast but accurate estimate of the storage requirements, given a high level C description as input?* A number of conference and journal papers were published presenting the results. I also developed a prototype CAD tool demonstrating the feasibility of the developed techniques. Based on this work I wrote and defended my Doctoral Thesis. It was also included as a chapter in a book published by Kluwer Academic Publishers describing the current status of the DTSE methodology. Parts of the DTSE methodology has since then been commercialized through the companies PowerEscape and CoWare.

After finishing my PhD, I was permanently employed as an Associate Professor at Department of Physical Electronics, NTNU (now part of Department of Electronics and Telecommunications). The first PhD-student I supervised, Qubo Hu, continued the cooperation with IMEC within the field of memory size estimation and optimization. Before successfully defending his thesis in April 2007, Hu had several prolonged stays at IMEC and also published several conference and journal papers. Currently the cooperation with IMEC is continued through the work of a new PhD-student, Elena Hammari. With her the direction changes somewhat as she will focus on utilization of computational resources in heterogeneous multi-processor system on chip. In addition to having me as supervisor and a co-supervisor from IMEC, Hammari also has Professor Lasse Natvig from Department of Information Technology and Computer Science, NTNU, as co-supervisor. Furthermore, her work is supported by the group working in the field of real-time systems at Department of Engineering Cybernetics, NTNU. This demonstrates the multi-disciplinary quality of the project, and its importance in various fields. In the memory optimization research area I also cooperate with Department of Information Technology and Media at Mid-Sweden University, Sweden.

In later years I have added techniques for optimized implementation of digital signal processing applications to my research interests. In 2003 I participated in writing the proposal for the CUBAN project (Co-optimized Ubiquitous Broadband Access Networks) together with the signal processing group at our department. The motivation for this project is the growing demand for wireless access to broadband services for mobile and nomadic users. It is expected that this demand will continue to increase in the years to come. The CUBAN initiative suggests the establishment of a ubiquitous wireless broadband access network based upon existing infrastructure. Three core activities (CA) have been defined. The first CA deals with using xDSL connections to a large number of WLAN access points in the fixed telecommunication network. The second CA deals with methods to analyze and optimize receiver performance under power limitations in battery-powered equipment. The third CA takes up the implication from the fact that the proposed network will only contain short range wireless links. This means that processing power in the terminals will be comparable to radiated power plus power dissipated in the transmitter. This situation calls for co-optimization over several disparate fields, such as modulation, coding, circuit design, and memory management. I am involved in the hardware/software implementation and optimization part of the project, and supervise PhD-students Saeed Tahmasbi Oskui and Asghar Havashki within this field. Parts of the work of both of them are performed in co-operation with the Electronics Systems division at Department of Electrical Engineering, University of Linköping, Sweden. Later I have also become involved in the CROPS project (CRoss-layer OPTimization in Short-range wireless sensor networks). Here I am co-supervisor for PhD-student Changmian Wang who works with co-optimization of link adaptation and resource allocation schemes and node circuitry power consumption.

In addition to the activities described above, I have participated in several internal and external projects in order to exploit our local research environment. A number of the master students I supervise have projects that are defined and co-supervised by industrial companies. This gives rise to a collaboration rewarding for both student and company. It also assists me in staying updated on topics seen as relevant by the industry, for use in both my teaching and research.

Between October 2005 and June 2006, I was a visiting researcher at Center for Embedded Computer Systems (CECS), University of California, Irvine. I was invited by Professor Nikil Dutt and participated in their memory and telecom related research. Since there is also a strong link between CECS and IMEC, I was also able to continue my cooperation with them.

In parallel with my research and supervision of PhD and Master Students, much of my time is devoted to giving lectures and coordinating activities in a number of courses. Each autumn semester since 2001 I have been responsible for a second year course in digital design and computer architecture. When I began it had more than 600 students. With five big laboratory assignments for each student, comprehensive theory assignments, 20 student assistants, and four

hours of lectures a week, this was a challenging task. I find this part of my work both interesting and rewarding and students in general give positive feedback regarding my teaching abilities. The 600 student course has recently been split, so that it now has a more manageable number of students (150-200). In addition to this, I teach (parts of) a third year course in digital systems design (introduction to VHDL, verification strategies, and logic synthesis), a fifth year course in HW/SW codesign, and a PhD course in memory optimization techniques. I am also involved in an Erasmus Mundus European Master Embedded Computing Systems program. This program is sponsored by the European Union (EU) and is organized as a cooperation between NTNU (departments at the IME faculty), University of Kaiserslautern, Germany, and University of Southampton, United Kingdom. I am deputy leader for the activities at NTNU.

As part of my job I also have a number of administrative duties. Currently, the main task is to be my department's member in the Board for research and researcher education at our Faculty. This board discusses research strategies at the Faculty level, handles PhD-student applications and progress, and in general functions as an advisory board for the Dean in research matters. This duty takes quite some time but gives good insight into research strategies as well as research politics. As secretary of Mikroelektronikkforum, a discussion forum with participation from our department and nine microelectronics companies, I lead its work with improved education quality and candidate production in this field as the goal. Outside the university I am (and have been) member of the board of directors of several companies. In two periods (1995-1999 and 2003-2007) I was member of the board of directors of my former employer, Eidsvoll Electronic AS. Currently I am also a member of the board of directors at Thelma AS (chairman between 2001 and 2009). This gives me experience in the challenges the industry faces, as well as in leading board work.

In September 2007 I applied for promotion to Professor based on acquired competence. A national committee, with assistance from two international experts, concluded that I fulfilled the requirements, and I became Professor in the field of "design and analysis of embedded hw/sw systems" in February 2009.